Global Scientific JOURNALS

GSJ: Volume 6, Issue 6, June 2018, Online: ISSN 2320-9186
www.globalscientificjournal.com

BASIC REVERSIBLE LOGIC GATES

Swati Sonawane, Proff. Vishal Puranik,

ME (E & TC) Dept JSPM's BSIOTR, Wagholi, Pune, India. Email: sonawaneswati16@gmail.com
Professor (E & TC) Dept JSPM's BSIOTR Wagholi, Pune, India. Email: vishalpura@gmail.com

KeyWords
Reversible logic, Fredkin Gate, Toffoli Gate, Parity Preserving Reversible Logic Gate

ABSTRACT

Reversible logic has obtained importance in recent times because of the fact that power consumption in these circuits can be drastically reduced. In conventional digital circuits, a significant amount of energy is dissipated as the bits of information are lost during logical operations. This loss of bits of information can be avoided by using reversible logic gates. This paper gives the valuable information of about the reversible logic gates designed and the circuits implemented using the same.

1. Introduction

Energy dissipation is of fundamental in the design and implementation of VLSI circuits. As the number of circuits integrated on a chip increases and the chip size decreases, energy dissipation thus becomes the greater area of important for designers. Conventional digital circuits dissipate a important amount of energy owing to loss of information. According to Landauer's research, the amount of energy dissipated for every irreversible bit operation is at least KTln2 joules, where K is the Boltzmann's constant and T is the temperature at which operation is performed [1]. The heat generated due to the loss of one bit of information is very small at room temperature but when the number of bits is more as in the case of high speed computational works the heat dissipated by them will be so large that it affects the performance and results in the reduction of lifetime of the components In 1973, Bennett showed that KTln2 energy would not dissipate from a system as long as the system allows the reproduction of the inputs from observed outputs [2]. Reversible logic supports the process of running the system both forward and backward. This means that reversible computations can generate inputs from outputs and can stop and go back to any point in the computation history. A circuit is said to be reversible if the input vector can be uniquely recovered from the output vector and there is a one-to-one correspondence between its input and output assignments, i.e. not only the outputs can be uniquely determined from the inputs, but also the inputs can be regain possession from the outputs. Energy dissipation can be reduced or even eliminated if computation becomes Information-lossless.

2. Concept

In computing, reversibility suggest that no information about the computational states can ever be lost and thus we can recover any earlier stage by computing backwards or un-computing the results. This is termed as logical reversibility. The benefits of logical reversibility can be obtained only after employing physical reversibility. Physical reversibility is a process that dissipates no energy to heat. Absolutely perfect physical reversibility is practically unachievable. Computing systems give off heat when voltage levels change from positive to negative: bits from zero to one. Most of the energy needed to make that change is given off in the form of heat. Rather than changing voltages to new levels, reversible circuit elements will gradually move charge from one node to the next. In this way, one can only expect to lose a minute amount of energy on each transition. Reversible computing is capable of exerting or resisting great power in digital logic designs. Reversible logic elements are needed to regain the state of inputs from the outputs. Eventually, these will also have to be reversible to provide optimal efficiency.

3. Motivation

Reversible circuits that conserve information, by uncomputing bits instead of throwing them away, will soon offer the only physically possible way to keep improving performance. Reversible computing will also lead to improvement in energy efficiency. Energy efficiency will fundamentally affect the speed of circuits such as nanocircuits and therefore the speed of most computing applications. To increase the portability of devices again reversible computing is required. It will let circuit element sizes to reduce to atomic size limits and hence devices will become more portable. Although the hardware design costs incurred in near future may be high but the power cost and performance being more dominant than logic hardware cost in today's computing era, the need of reversible computing cannot be ignored. Design constraints for reversible logic circuits [4]:

- Reversible logic gates do not allow fan-outs.
- Reversible logic circuits should have minimum quantum cost.
- The design can be optimized so as to produce minimum number of garbage outputs.
- The reversible logic circuits must use minimum number of constant inputs.
- The reversible logic circuits must use a minimum logic depth or gate levels

A reversible logic gate is an n-input and n-output logic device with one-to-one mapping [3]. Reversible logic gates helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. Also in the synthesis of reversible circuits direct fan- Out is not allowed as one–to-many concept is not reversible. However fan-out in reversible circuits is achieved using additional gates. A reversible circuit should be designed using minimum number of reversible logic gates. There are many parameters for determining the complexity and performance of circuits.

- Number of Reversible gates (N): The number of reversible gates used in circuit.
- Number of constant inputs (CI): This refers to the number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function.
- Number of garbage outputs (GO): This refers to the number of unused outputs present in a reversible logic circuit. One cannot avoid the garbage outputs as these are very essential to achieve reversibility.
- Quantum cost (QC): This refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit.

4.1 Basic Types of Reversible Logic Gates

4.1.1 Toffoli Gate

The below figure shows the block diagram of Toffoli gate. The circuits have 3 inputs and 3 outputs. The input vector is I(A, B, C) and the output vector is O(P,Q,R). The outputs are defined by P=A, Q=B, R=AB EXOR C. Quantum cost of a Toffoli gate is 5.

Fig 1: Toffoli Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

Table 1- Truth Table of Toffoli Gate

4.1.2 Fredkin Gate

The below figure shows the block diagram of Fredkin gate. The Fredkin gate has 3 inputs and 3 outputs. The input vector is I (A, B,C) and the output vector is O (P, Q, R). The output is defined by P=A, Q=A'B⊕AC and R=A'C⊕AB. Quantum cost of a Fredkin gate is 5.

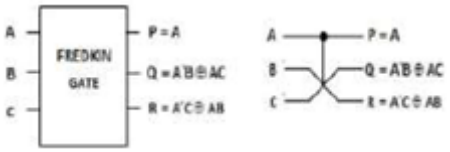

Fig. 2 Fredkin Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

Table 2- Truth Table of Fredkin Gate

4.1.3 MIG Gate

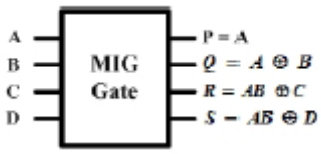

Fig. 3 4*4 MIG Gate

The above figure shows the diagrammatic representation of MIG Gate. The MIG Gate has 4 inputs and 4 outputs.

4.1.4 NCG (Nines compliment gate)

The most important feature of this NCG is when control signal E is equal to zero, four bit binary number is directly passed to the output Q, R, S and T .When E is equal to one then, Q, R, S and T is equal to nines compliment of the number A,B, C and D. Therefore depending on control signal E, either passnine's compliment outputs will be available on output Q, R, S and T.

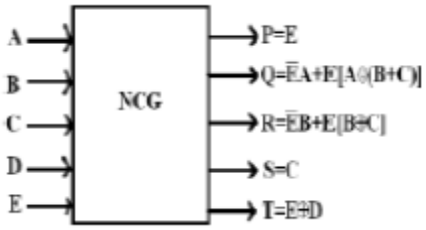

Fig. 4. NCG (Nines compliment gate)

4.1.5 Parity Preserving Reversible Gate (P2RG)

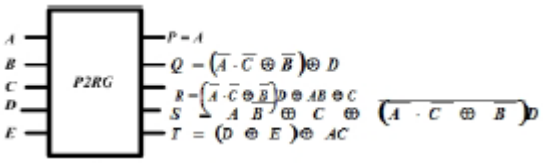

Fig. 5: (a) 5*5 parity preserving reversible gate (P2RG)

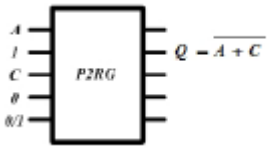

Fig.5: (b) P2RG as universal gate

The above figure shows the parity preserving reversible gate. I t has 5 inputs and 5 outputs. P2RG is also used as a universal logic gate.

5. Results

Reversible Logic gate	No of Slices LUTs Used	No of Shift Registers LUTs Used
TG	1	1
FRG	2	2
MIG	3	3
NCG	3	3
P2RG	4	4

Table 3. Area Utilization of Different Reversible Logical gates

Reversible Logic gate	Combination Path Delay
TG	5.38 ns
FRG	5.456 ns
MIG	5.456 ns
NCG	5.505 ns
P2RG	5.520 ns

Table 4. Time Analysis of Different Reversible Logical Gates

6. RTL Schematic

The below figures shows the RTL Schematic of various reversible logic gates.

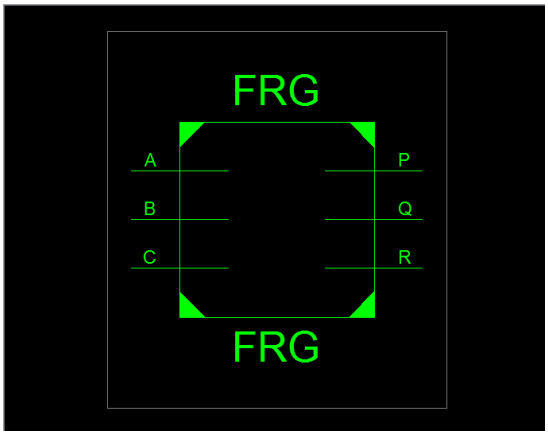

Fig.6 RTL Schematic of Fredkin Gate

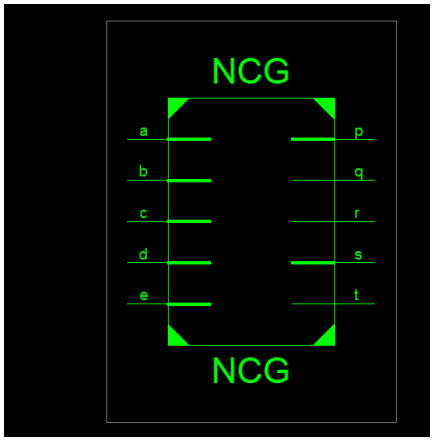

Fig.7 RTL Schematic of NCG Gate

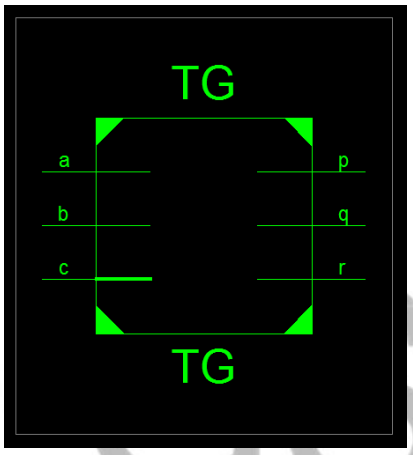

Fig.8 RTL Schematic of Toffoli Gate

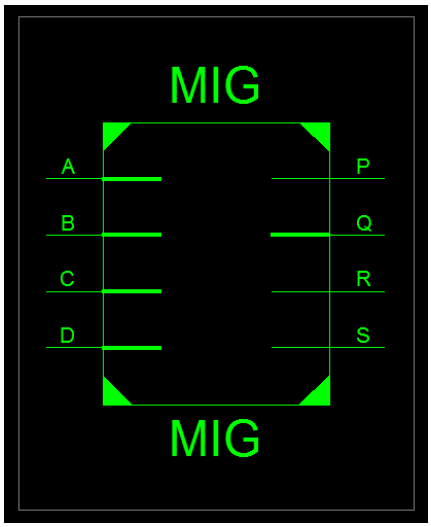

Fig.9 RTL Schematic of MIG Gate

Fig.10 RTL Schematic of Parity Preserving Reversible Gate

7. Testbench Waveforms

The below figures shows the test bench waveform of various reversible logic gates.

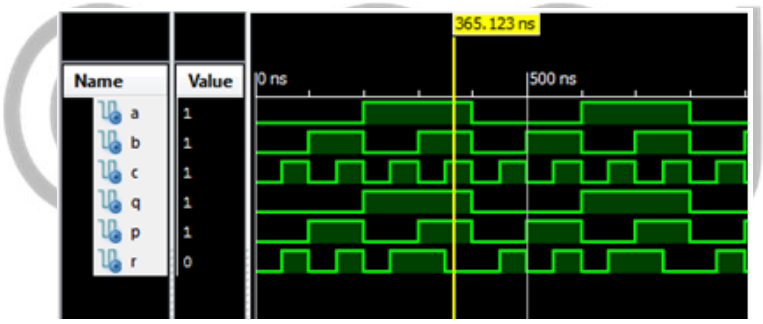

Fig.11 Testbench wavewform of Toffoli Gate

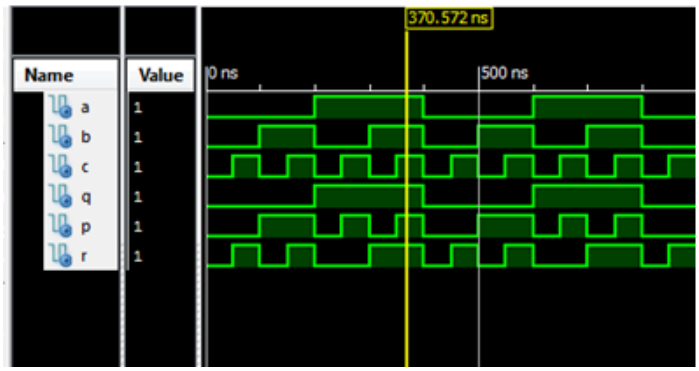

Fig.12 Testbench wavewform of Fredkin Gate

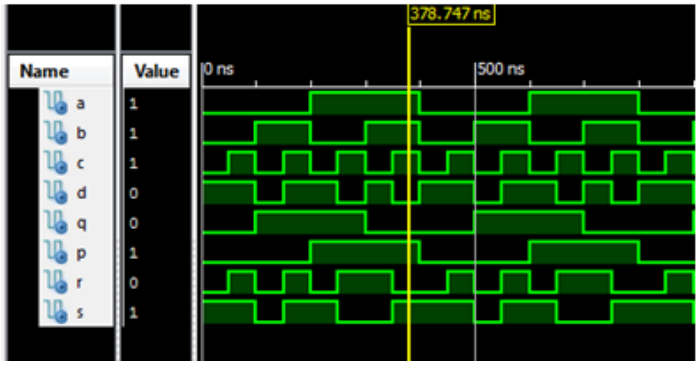

Fig.13 Testbench wavewform of MIG Gate

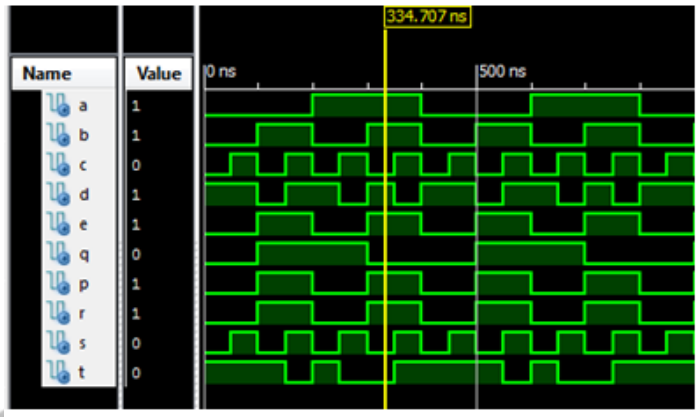

Fig.14 Testbench wavewform of NCG Gate

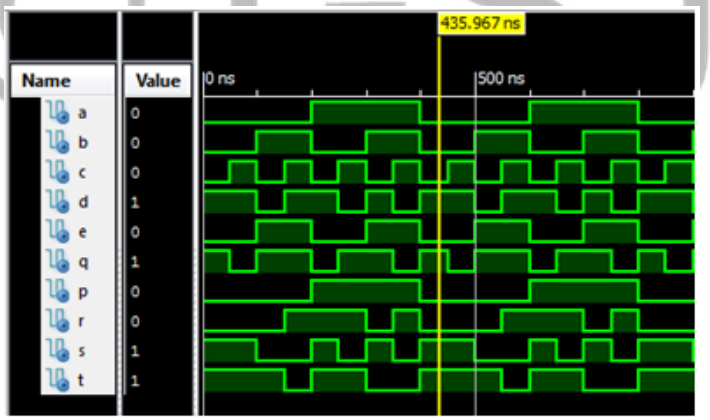

Fig.15 Testbench wavewform of P2RG Gate

8. **Conclusion**

Reversible logic gates form the building blocks of quantum computing. This paper gives an overview of the reversible logic gates gathered from literature surveys. This paper can be further extended towards development of circuits using these primitive gates.

Acknowledgment

I am very thankful to Prof. Vishal Puranik for his valuable support and guidance for making this project successful.

References

[1] [1] Landauer, R., "Irreversibility and heat generation in the computing process", IBM J. Research and Development, 5(3): pp. 183-191, 1961.
[2] [2] Bennett, C.H., "Logical reversibility of Computation", IBM J.Research and Development, 17: pp. 525-532, 1973.
[3] [3] Prashant .R.Yelekar, Prof. Sujata S. Chiwande, "Introduction TO Reversible Logic Gates & its Application", 2nd National Conference on Information and Communication Technology (NCICT) 2011, Proceedings published in International Journal of Computer Applications® IJCA,2011.
[4] [4] Raghava Garipelley et al., "A Review on Reversible Logic Gates and their Implementation", International Journal of Emerging Technology and Advanced Engineering, Volume 3, Issue 3, March 2013.
[5] [5] Madhusmita Mahapatro et al., "Design of Arithmetic Circuits Using Reversible Logic Gates and Power Dissipation Calculation", Proceedings in International Symposium on Electronic System Design, pp 85-90, 2010.
[6] [6] Asima Jamal et al., "Design of Low Power Counters using Reversible Logic", International Journal of Innovative Research in Science, Engineering and Technology, Volume 3 Issue 5, May 2014.
[7] [7] Rashid Anwar et al., "A Novel Design of Reversible Universal Shift Register", International Journal of Computer Science and Mobile Computing, Vol. 3 Issue 3, pp 530-535, March 2014.
[8] [8] Md. Belayet Ali et al. "Design of Reversible Sequential Circuit Using Reversible Logic Synthesis", International Journal of VLSI Design &
[9] Communication Systems (VLSICS) Vol.2, No.4, Dec