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Design and implementation of memory cells in digital electronics

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Abstract

CMOS technology feature size and threshold voltage have been declining for decades to achieve high density and high performance. Increased chip density and operating frequency have made power consumption a major concern for the VLSI design. This paper provides Static Random Access Memory (SRAM) frameworks for low power dissipation with 6T AND 8T SRAM, Random Access Memory (DRAM) flexible and Filp-flop. Powerful random access memory is one of the most important components of a computer program, and today thanks to technological advances in many other programs. The development of this memory is very important because its development affects the performance of the programs in which it is used, and that is one of the main reasons why it should be analyzed and studied. Flip flop has minimal space and low power consumption which can be used in various systems such as VLSI digital clock system, baths, registers, microprocessors etc.

1. INTRODUCTION

Digital electronics and Memory cells

In digital electrical circuits, electrical signals take different values, representing rational and numerical values. These figures represent the information being processed. In most cases, the binary code text is used: one voltage (usually the best value) represents binary '1' and the other voltage (usually the nearest value to low power, 0 V) stands for binary '0'. Digital circuits make extensive use of transistors, connected to create intelligent gates that provide Boolean logic functions: AND, NAND, OR, NOR, XOR and your combinations. Transistors connected to provide constructive feedback are used such as latches and flip flops, circuits with two or more metastable shapes, and remain in one of these circuits until the external inputs are replaced. Digital circuits can therefore provide insight and memory, enabling them to perform random computer tasks. Flip-flops based memory is known as random access memory (SRAM). Capacitor-based memory, random access memory (DRAM) is also widely used.

The process of designing digital circuits is very different from the process of analog circuits. Each sensible gate generates a binary signal, so the designer does not have to respond to distortion, gain control, exchange power, and other concerns encountered in the analog architecture. As a result, highly sophisticated digital circuits, with billions of sensible materials combined with a single silicon chip, can be built at low cost. Such integrated digital circuits are found everywhere in modern electronic devices, such as counters, laptops, and computers. As digital

circuits become more complex, time-delayed problems, sensible races, power outages, incorrect switching, chip and inter-chip loading, and leakage of currents, become limitations in circuit breakdown, speed and performance.

Digital circuitry is used to create custom computer chips, such as microprocessors, and intelligently designed circuits, known as application-specific integrated circuits (ASICs). Fixed gate arrays (FPGAs), chips with logic circuitry configurations can be modified after processing, and widely used for prototyping and development. In computer history, a variety of memory cells have been used, including contextual memory and bubble memory. Today, the most common memory cell formation is MOS memory, which contains iron-oxide-semiconductor (MOS) memory cells. Modern random access memory (RAM) uses MOSFETs (MOSFETs) as flip-flops, as well as MOS capacitors for certain types of RAM. The SRAM (static RAM) memory cell is a type of flip-flop circuit, commonly used with MOSFETs. This requires very little energy to keep the amount accessible. The second type, DRAM (variable RAM), in this charging and discharging capacitor can store '1 'or' 0 'in a cell. However, charging in this capacitor will leak slightly, and should be renewed from time to time. As a result of this regeneration process, DRAM uses more energy. However, DRAM can reach a large final capacity.

On the other hand, most stationary memory (NVM) is based on the formation of floating memory cells. Flexible memory technologies that include EPROM, EEPROM and flash memory use floating gate memory cells, supported by MOSFET transistors at the floating gate. A memory cell is the basis for building memory. It can be used using a variety of technologies, such as bipolar, MOS, and other semiconductor devices. It can also be made of magnetic materials such as ferrite cores or magnetic bumps. Saves binary data in 0s and 1s.

2. SIGNIFICANT

Sensible circuits that do not have memory cells or response mechanisms are called combinations, output values depending on the current value of their input values. They have no memory. But memory is the most important unit of digital programs. On computers, it allows the storage of both systems and data. These memory cells are also used for temporary storage of integrated circuits that will later be used by digital systems. Sensible circuits that use memory cells are called consecutive circuits. The output depends not only on the current value of the input, but also on the previous state circuits, as determined by prices. These circuits require a time generator or a clock to operate.

The computer memory used in most current computer programs is primarily made up of DRAM cells; as the format is much smaller than SRAM, it can be very compact and provide cheap memory with a large capacity. As the DRAM memory cell retains its value as a capacitor charge, and there are current leakage problems, its value must be rewritten regularly. This is one of the reasons why DRAM cells are slower than large SRAM cells (standing RAM), their ever-present value. This is why SRAM memory is used in an on-chip storage mounted on modern microprocessor chips.

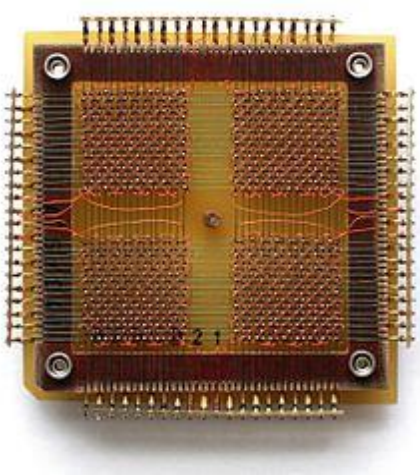


Fig 1: 32x32 is a master memory aircraft that stores 1024 bits of data.

3. HISTORY

On December 11, 1946, Freddie Williams applied for a patent on his cathode-ray (CRT) (Williams tube) storage device containing 128 40-bit words. It was operational in 1947 and is considered an effective implementation of random access memory (RAM). The working memory was invented by An Wang in 1948, and developed by Jay Forrester and Jan A. Rajchman in the early 1950s, before being sold by Whirlwind in 1953. Ken Olsen also contributed to its development.

Semiconductor memory began in the early 1960's with bipolar memory cells, made up of bipolar transistors. Although it improved performance, it was not able to compete with a low level of magnetic memory.

4.MOS MEMORY CELL

MOS memory and random access memory § History

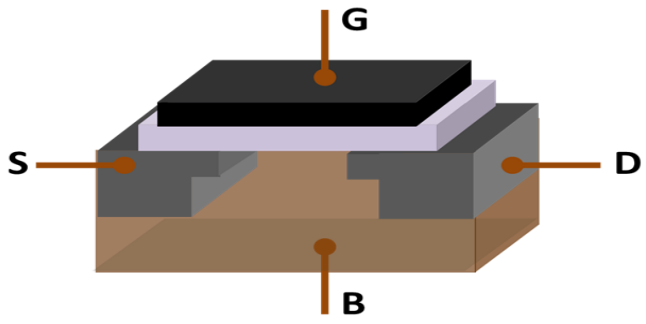


Fig 2: Intel 1103, 1970s metal-oxide-semiconductor (MOS).

A major advantage of MOSFE is MOSFET (metal-oxide-semiconductor field-effect transistor) s in digital transitions that the oxide layer between gate and channel prevents current DC from flowing through the gate, and reduces power consumption and provides greater efficiency. input resistance. The protective oxide between the gate and the channel effectively separates MOSFET from a single thinking phase from the previous and a

recent phase, allowing a single MOSFET outlet to drive a large amount of MOSFET input. Bipolar transistor-based logic (similar to TTL) does not have such a large fanout capacity. These differences make it easier for designers to ignore the effects of loading between sensible sections independently. That level is defined by the frequency of operations: as the frequency increases, the interruption of MOSFET installation decreases.

The invention of the MOSFET also known as the MOS transistor at Bell Labs in 1959, led to the successful use of metal-oxide - semiconductor (MOS) transistors as the endothelial cells of memory, a function previously assigned to magnetic core.

SRAM usually consists of six alternating cells, while DRAM (random memory for random access) usually contains single transistor cells. In 1965, Toshiba's Toscal calculator BC-1411 used a capacitive bipolar type. DRAM, stores 180-bit various data. memory. cells, including germanium bipolar transistors and capacitors. MOS technology is the basis of modern DRAM.

The two most common types of DRAM memory cells are trench-capacitor cells and capacitor memory cells. , while stacked capacitor cells are the first type of three-dimensional memory (3D memory), in which the memory cells are packed directly into a three-dimensional cell structure.

Enhanced MOS Capacitor

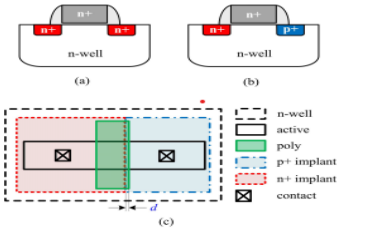


Fig 3: Transverse components (a) of a standard MOS capacitor and (b) an upgraded MOS capacitor. (c) Composition of improved MOS capacitor.

In the normal CMOS process, a device with an n-type gate is usually paired with n-type junctions, and thus a standard MOS capacitor contains a n-type gate, a n-junction, and a n-source. By replacing the p + input of the n + input beyond the operating side side, we get an upgraded MOS capacitor. Compared to a standard MOS capacitor, the upgraded MOS capacitor has both n-type and p-type channels, which can provide the channel with enough holes as soon as the capacitor is pressed by the wrong sweep ramp, and this will prevent the capacitor . from a state of deep decay. On the other hand, a standard MOS capacitor can only produce holes in the channel through thermal production processes, in this case very slow motion. Therefore, the reduction layer continues to grow above its maximum temperature value in order to balance the negative gate charge, resulting in greater local power and less power than ratings. In fact, an upgraded MOS capacitor may be subject to the unbalanced effect of n + insertion and p + insertion, which will affect the gate, and that will ultimately lead to significant cell power distribution (VTH). To solve the problem, there are two design elements that need to be carefully considered, namely, the length of the spaces between the p + installation layer and the poly layer, and the channel length. Considering the actual effect of misalignment on the normal CMOS process of 0.13-µm, we set the d to 50 nm and the minimum channel length to 0.5 µm. Finally, most polyarea is n + n, which brings the

device and gate functionality to the wrong polarity [20], and the channel is long enough to release the effect of misalignment. In addition, a spacing of 50 nm ensures adequate drainage of the p-type, and thus produces the required p-type junction near the track. It is noteworthy that the upgraded MOS capacitor is fully compliant with the normal CMOS process, and is less than the 0.13-µm CMOS process without any additional mask or processing steps in this paper.

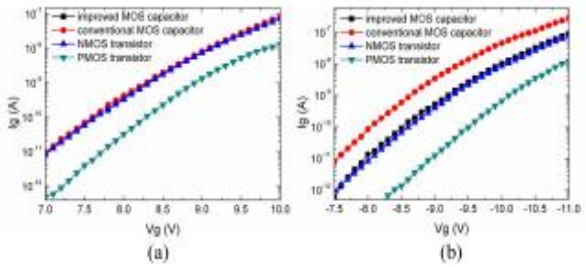


Fig 4: Measurement of gate flow of different instruments (a) in positive polarities and (b) negative. Source, drain, and bulk devices are ground-based, and the channel size of all test devices is 1 µm × 1 µm.

Figure 4 shows a comparison of the current gateway between an upgraded MOS capacitor and other devices, including a standard capacitor, NMOS transistor, and PMOS transistor, both positive and negative. According to Fig. 4, the PMOS transistor has the lowest current in both polarities, and the upgraded MOS capacitor has the same current as the standard capacitor and NMOS transistor at good polarity, and the NMOS transistor with negative polarity . These results are consistent with the conclusions in. However, as shown in Fig. 4 (b), the current gate of a standard capacitor is three to seven times larger than the capacitor developed at the wrong polarity. This is really interesting, and the strength of the collision is considered to be a reflection of the great impact that occurs on a normal MOS capacitor. Due to the limited source of channel holes and reconnection with electrons installed in the gate, a standard capacitor is still much wider than an enhanced capacitor in negative and normal irrigation mode, and thus in a standard capacitor, gate electrons will receive. sufficient power to make the electron-hole pairs are important in the reduction area, and the new holes produced will be injected opposite the gate, thus resulting in greater gate strength. However, it is important to note that in a stable case the normal capacitor has a large negative current, while the low, current voltage will be much lower as there are fewer electrons pulling at the gate to initiate the avalanche.

Floating MOS memory cells

MOSFET floating gate and unmistakable memory

The floating gate MOSFET (FGMOS) was founded by DawonKahng and Simon Sze at Bell Labs in 1967. They suggest the concept of floating gate memory cells, using FGMOS transistors, which can be used to produce compact ROM (read-only memory). Floating gate memory cells later became the basis for static memory (NVM) technologies including EPROM (removable formatable ROM), EEPROM (removable removable ROM) and flash memory.

Flash Memory was founded by Fujio Masuoka at Toshiba in 1980. Masuoka and colleagues introduced the launch of the NOR flash in 1984, and then the NAND flash in 1987. 64 Mb flash chip cells retained 2-bit cells in 1996.3D V-NAND, when flash memory cells accumulated directly using 3D charge trap flash (CTP) technology, first introduced by Toshiba in 2007 , and began commercial production by Samsung Electronics in 2013.

Implementation

The following schemes contain details of the three most commonly used memory cells:

• Random access memory (DRAM)

• Random access memory (SRAM) cell

• Flip-flop like the J / K shown below.

5.DRAM MEMEORY CELL

As the term DRAM, or random variable access memory, suggests, this type of memory technology is a type of random access memory. It stores each data in a small capacitor inside a memory cell. A capacitor can be charged or discharged and this provides two circuits, cell "1" or "0".As charging inside the capacitor leaks, it is necessary to refresh each memory cell periodically.This renewal requirement creates the word dynamic - static memories do not need to be renewed.

The advantage of DRAM is the simplicity of the cell - it requires only one transistor compared to six in standard RAM, the SRAM memory cell. Given its simplicity, DRAM costs are much lower than those of SRAM, and are able to provide much higher levels of memory congestion. DRAM, however, is also bad, and as a result, many computers use both DRAM and SRAM technology, but in different areas.

Considering the fact that power is needed for DRAM to store its data, this is called dynamic memory. Memory technologies such as Flash are flexible and retain deleted data or power

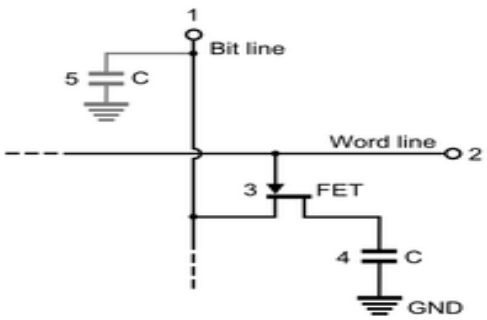


Fig.5: DRAM cell (1 transistor and one capacitor)

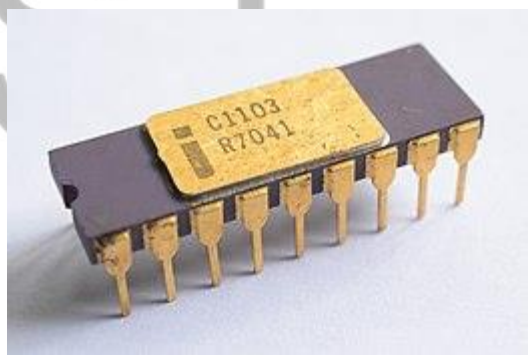


Fig 6: DRAM chip

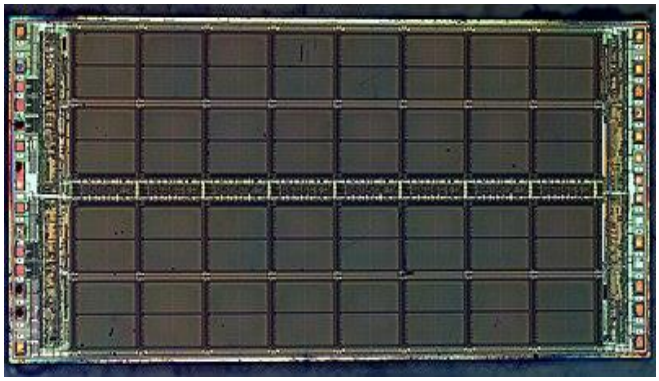


Fig.7: Die of the MT4C1024 (1994) which combines a single mebibit of DRAM memory cells.

Storage

The last part of the DRAM memory is the capacitor labeled (4) in the diagram above. The charge stored in the capacitor decreases over time, so its value must be renewed (read and rewritten) from time to time. The nMOS transistor (3) acts as a gateway that allows reading or writing when turned on or stored when closed.

Reading

To read the Word line (2) you drive logic 1 (high voltage) at the gate of the nMOS transistor (3) which makes it smooth and the charge is stored in a capacitor (4) and transferred to the bit line (1). The thin line will have a parasitic power (5) that will drain the charging component and slow down the learning process. The smaller line capacity will determine the required size of the final capacitor (4). Trading. If the final capacitor is too small, the voltage of the thin line will take too long to increase or not increase even beyond the limit required by the amplifiers at the end of the thin line. As the learning process lowers the charge on the last capacitor (4) its value is rewritten after each reading.

Types of DRAM

DRAM memory is just one type of RAM. And within the DRAM category, there are a few types you should be aware of.

1. SDRAM

Synchronous DRAM, or SDRAM, improves performance with its anchors, which improves the data connection between the microprocessor and the primary memory.

2. DDR SDRAM

DDR SDRAM has SDRAM features, but the frequency of data transfer is doubled. So it is called as "double data rate SDRAM."

3. ECC DRAM

This type of DRAM can detect corrupted data and sometimes repair it, due to its error correction code (ECC).

4. DDR2, DDR3, and DDR4

Most HP computers use the DDR series of DRAM chips. Technology is evolving from one generation to the next, which is reflected in a series of numbers. DDR4, for example, is faster and more efficient than DDR2 or DDR3.

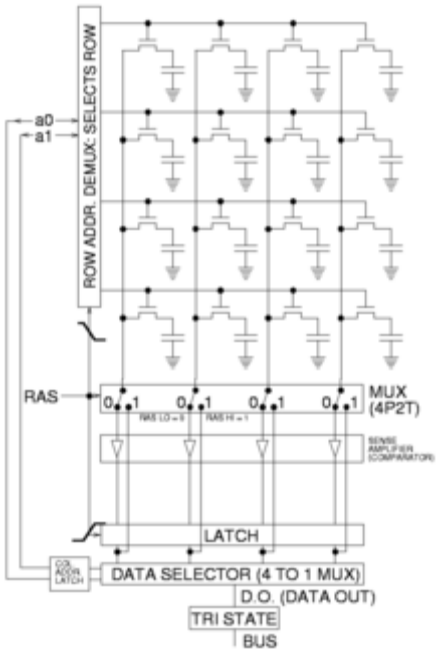


Fig.8: Square list of readable DRAM memory cells

6. SRAM MEMORY CELL

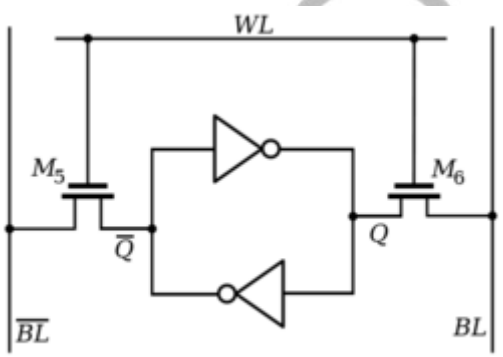


Fig.9: SRAM memory cell showing Inverter Loop as gate

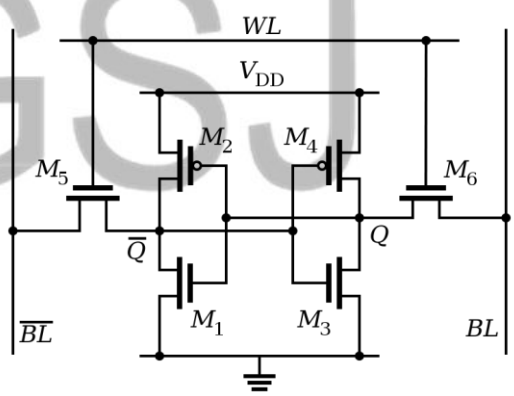


Fig.10: Agreement 6T SRAM

Storage

The operating principle of the SRAM memory cell can be easily understood when transistors M1 to M4 are designed as sensible gates. Thus it is clear that at its heart, cell storage is built using two integrated inverters. This simple loop creates a bi-stable circuit. Logic 1 in the first converter input turns 0 at its output, and is inserted into the second converter that converts that logic 0 back to logic 1 returns the same value in the first converter input. That creates a stable environment that will not change over time. Similarly another stable state of the circuit having 0 logic in the inverter installation first. After it is twisted twice it will answer the same number.

There are therefore only two stable circuits in which the circuit can be located:

• Q = 0 and Q ’= 1

• Q = 1 and Q ’= 0

Reading

To read the stored data transistors M5 and M6 must be turned on. when the voltage flows to their gates from the word line values are transferred to the bit .Finally these values are amplified at the end of a small line.

Writing

The typing process is the same, the difference is that now a new value that will be stored in the memory cell is driven into the bit line (BL) and converts one into its complement (BL ’). The following transistors M5 and M6 are opened by dialing one logic (voltage high) in the word line (WL). This effectively connects the bit lines to the by-stable inverter loop.

Suggested 8T SRAM:

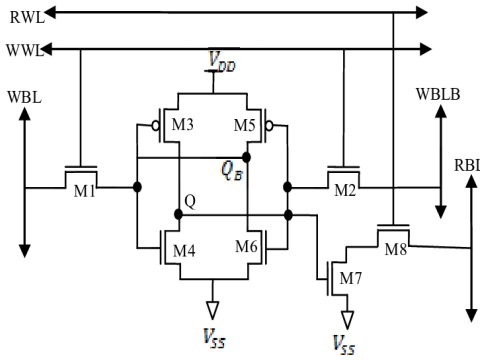


Figure .11: 8T SRAM proposed

It is noteworthy that in a related SRAM cell, the specified type of operation is usually set to the correct voltage line selection. However, this involves additional edge circuits such as bit line circuits and writes drivers to perform the correct part of the line power before any operation. When the ground provides voltage due to 6T SRAM cellular noise limits we usually use 8T SRAM cell in fast transmission systems. similar to a 6T SRAM cell with a separate scanning system that combines M5 and M6 transistors. Let’s take a look at the performance of the 8T SRAM style.

DESIGN AND PERFORMANCE OF 8T SRAM 4 BITS MEMORY CIRCUIT

To use 4 bit SRAM memory use 2-4 line decoders and 2-4 column decoders. It is organized in 4x4 matrixes (SRAM 8T cell) form. Here the output of the row decoder is connected to the SRAM “WL” cell name line and the sub-lines of all cells are connected to the column codec. When the input codec is 00, the first word “WL” line is at the top and all SRAM cells are connected in a small line. But depending on the address of the column decoder one column will be selected. This way a specific SRAM memory list cell will be selected. For example, if "00" will be your address for both the row decoder and the column decoder, then a specific cell with a "00" in its memory will be selected. If the line decoder address is “00” but the column decoder address is “01” then a second SRAM cell of the first row is selected.

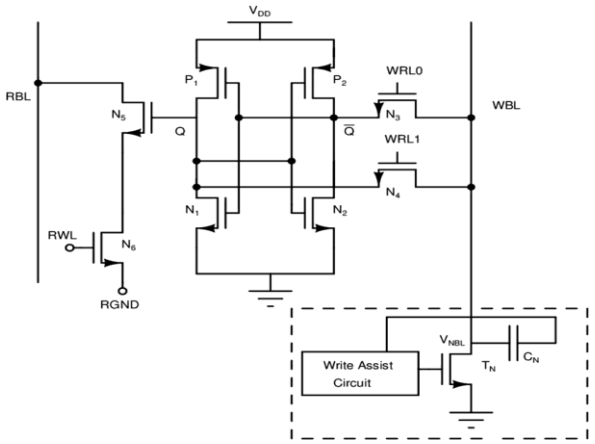


Fig.12: Designing and implementing an 8t SRAM 4-bit memory circuit

MEMORY UNIT 8T SRAM Memory design requires open circuits

1. Write the driver

2. charging

3. Sensor amplifier

4. decoder

The decoder is used to enable each memory cell that stores one piece of data. Pre-charge is used to store bit line and bit web line to vdd after all flip-flop Memory cell

The flip-flop has many different launches, the last part of which is usually a latch that includes a NAND gate loop or NOR gate loop with additional gates used to install the clock. Its value is always available to read as an output. The value remains kept until it is changed through the reset or reset process. Flip-flops are usually operated using MOSFET transistors.

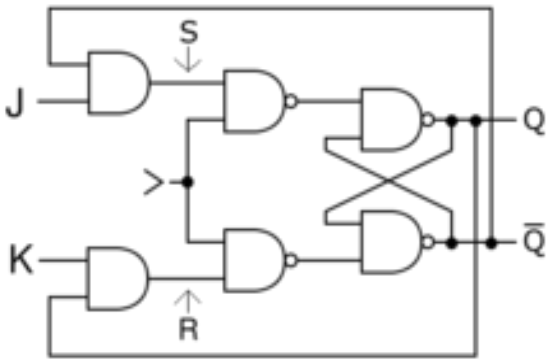
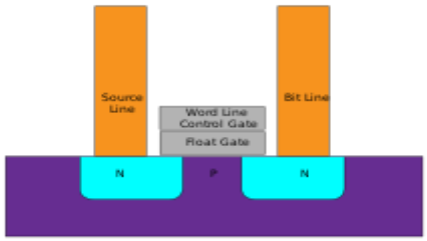


Fig .13: Flip-flop clock J / K

Floating gate memory cells, based on MOSFET floating transistors, are used for a variety of fixed memory (NVM) technologies, including EPROM, EEPROM and flash memory.

According to R. Bez and A. Pirovano: The floating gate memory cell is basically an MOS transistor with a floating gate dielectrics (FG), and an integrated control gate (CG). As it is separated electronically, the FG acts as the storage electrode for the mobile device. The charge included in the FG is stored there, which allows the 'visible' voltage switch (i.e. VT seen in CG) of the cell transistor.

7. FLOATING GATE



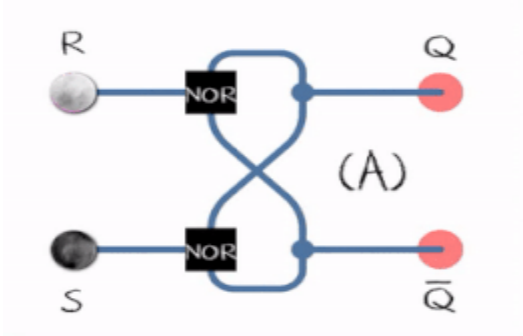


Fig.14: Flash memory cell

Very high number of SRs. Black and white means logical '1' and '0 ', VBrespectively.

(A) S = 1, R = 0: set

(B) S = 0, R = 0: hold

(C) S = 0, R = 1: reset

(D) S = 1, R = 1: not allowed

Switching from a limited combination (D) to (A) leads to an unstable state operations.

8. CONCLUSION

The SRAM 8T cell uses less power compared to the 6T transistor SRAM cell as the temperature rises. SRAM 8T cell transistor SRAM consumes less energy with different volumes of power supply compared to SRAM 6T cells. As the supply voltage down the power dissipation decreases. The 8T transistor SRAM consumes less power on the bit-line capacity compared to the SRAM 6T transistor. 4bit memory unit used. Although the SRAM voltage mode has been shown to be beneficial in reducing switching power, the overhead is local due to the addition of two other transistors and power sources. But this process can best be used where low power is directed. The 5T cell looks good in terms of location, performance but the top goes with the complexity of the design. Further research can be done by combining these strategies to achieve both low and beneficial variable results.

In this paper, we have studied how Dynamic Random Access Memory (DRAM) works. The role that this memory plays is critical to computer performance. Memory stores all data in a special capacitor within an integrated circuit. The capacitor may be full or empty; these two circuits are two-digit numbers, often called 0 and 1. As capacitors leak charging, the information will eventually disappear if the capacitor can be renewed from time to

time. As a result of these renewal requests, the variable memory conflicts with SRAM and other static memory. Powerful RAM memory does not have the speed of cleaning the processor in terms of performance, i.e. providing certain data at times when the processor needs it. This leads to the emergence of delays. In order not to waste time there are procedures in which the memory "deceives" the processor and avoids bringing the processor into full play mode. Another drawback is the appearance of errors in variable RAM memory. However, with different diagnostic and correction methods, many errors are prevented, or in the event of an error being corrected. The flexible RAM market changes from year to year depending on demand. Due to the emergence of NAND flash memory, the flexible RAM market has declined slightly, but apart from this it is recovering due to the high demand for later generation memory (DDR4, GDDR5, LPDDR4). Over time, memory grows faster and manufacturers try to produce memory that will have a speed closer to the processor's speed. In this paper, a complete analysis and design of the topology of flip-flops commonly used in 90mm CMOS technology has been performed.

9. FUTURE SCOPE

In order to perform a scripting task in a SRAM cell to convert the amount of data, approximately full power fluctuations are required in the bit line. This full voltage switches for very strong bit lines will use a large amount of power in terms of CV2 f. Reducing energy conversion is thus an effective way to reduce energy consumption. The future course includes effective reduction of leakage in the SRAM cell. Here it is proposed to develop appropriate methods to reduce leaks with an emphasis on reducing gate leaks. Reduced leakage in SRAM can also be done using a self-control button either at the end of the cell to lower the supply voltage (USR system) or at the lower end of the cell to raise ground power node (LPR scheme). This method will be re-evaluated for its effectiveness once the function has been upgraded.

The DRAM cell is made up of an access transistor and a capacitor. Data is stored in a capacitor as an electric charge, but electrical power leaks over time. Therefore, DRAM must be updated periodically to preserve the database.

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