Global Scientific JOURNALS

GSJ: Volume 9, Issue 1, January 2021, Online: ISSN 2320-9186
www.globalscientificjournal.com

Design and simulation of a lookup table based inverter for photovoltaic application

Muhtar H.Alhassan *

Department of Computer Science, National Open University of Nigeria
Abuja - Nigeria
* malhassan@noun.edu.ng

***Abstract*—This paper describes the design of a low-power, current-regulated three-phase inverter suitable for a solar photovoltaic drive using a synchronous permanent-magnet motor. Precise stator-current control is required to operate the machine in a self-synchronous mode. The general features aimed for in the design included, near-sinusoidal output current wave shape, variable output frequency in the range from rated down to DC, variable output amplitude; minimum losses, low noise generation together with compact and low inductance design.**

I. Introduction

The inverter presented is a current-regulated three-phase type suitable for a solar photovoltaic powered ac drive. The drive motor is a synchronous permanent magnet motor to be operated in the self-synchronous mode which requires precise *stator-current* control. The main features of the design included, near-sinusoidal output current wave shape; variable output frequency in the range from rated down to DC; variable output amplitude; minimum switching and other losses; minimum noise generation; compact and low inductance design.

To eliminate torque-pulsations and cogging effects at low speed, low harmonics must be removed from the output current of the inverter. This demand for a near-sinusoidal output rules out the simple six-step approach and necessitates the use of some form of pulse-width modulation (PWM). Furthermore, a square-wave PWM is unsuitable as it contains not only low-order harmonics but also additional high-frequency components introduced by switching. The block diagram of the proposed micro controller (Arduino)-controlled system is shown in **figure1**.

II. Design Specifications

The role of a motor is to create mechanical energy out of another form of energy. So its power output is derived from its maximum energy transformation capacity. In the case of an electric car, its power output depends on the size of its motor (its volume) and the wattage of the incoming current. So the battery's storage capacity and the power electronics that drive the motor affect its power output. Power output is also a result of yield, i.e. the quantity ratio of incoming electricity supplied to outgoing mechanical energy delivered.

The aim consists then in reducing power output losses caused by heat or friction to achieve maximum energy efficiency. This way, most of the energy stored in the battery is used to extend the vehicle's range.

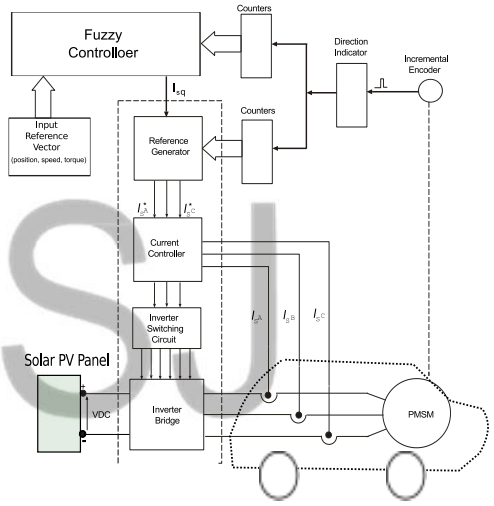

Fig. 1. *Block diagram of the Inverter-Motor System*

The maximum power output does not directly affect the range of an electric vehicle, since driving style has the greatest impact on the motor's consumption. For example, sharp acceleration will mean a spike in electricity consumption. Periods of high-speed driving also draw on the battery significantly. The higher the speed, the more energy is needed to sustain it.[2] Conversely, relaxed driving keeps instant consumption down and makes regenerative braking more effective. This is the principle behind eco-driving, which is one of the best ways to increase the range of an electric vehicle.

The battery capacity determines the range of the vehicle. Measured in kilowatt hours (kWh), the capacity represents the amount of energy available to power the engine and the different onboard equipments. Thus, a battery of capacity of 41 kWh enables a vehicle to travel up to 300 km in real conditions according to the WLTP (Worldwide Harmonised Light Vehicle Test Procedure), the latest standard for type approval testing of electric cars.[2]

In practice, the range really observed on a day-to-day basis varies depending on different factors. Some, like the outside temperature, are purely contextual: the range of an electric

car will be slightly lower in the harmattan season because the lower temperature can temporarily affect the battery's capacity.

Others depend entirely on the decisions of the user and their driving style. By being attentive to this handful of parameters, you can get more control over your electric car's consumption and therefore extend its range.

1) Nominal Values: Based on the expected operating condition of the inverter the following rated values were specified for the design

Item	Value	Unit
Power rating	2.5	kW
DC inputvoltage	48	volt
Output frequency range	0 to 33	Hz
Output current (max)	65	A

TABLE I
Inverter rated values

A. Performance Specifications

The general features aimed for in the design included

- Near-sinusoidal output waveshape
- Variable output frequency in the range from rated down to dc
- Variable output amplitude
- Low sensitivity to sudden surges of voltages and currents during normal operation
- Minimum switching and other losses
- Minimum noise generation
- Compact low-inductance design

III. Modulation Technique

The main strategy for controlling the motor is based on hysteresis current control. Thus digitally generated sine reference waves of variable frequency (from rated to zero and vice versa) are continuously compared with the actual *motor currents* within a small hysteresis band. The outcome of this comparison is used to determine the firing pattern of the inverter's power transistors. A look-up table approach is used to implement the sine reference generator and this eliminates the usual problems of *DC-offset* and *parameter-drift* that are characteristic of analogue sine-wave generators.

IV. Reference Generator

In the look-up table approach, the sine wave reference is stored in a table implemented in ROM and accessed at the rotor's frequency using rotor position signal from an incremental encoder. The sine wave is recovered using a multiplying DAC thus enabling amplitude variation. The block diagram of the reference generator is shown in **figure 2**.

The amplitudes of a **unit** sinewave are stored at regular angular intervals in the form of a digital look-up table in read-only-memory (ROM). The encoder-generated pulses f_i are used to clock the programmable up/down counter, which generates the ROM address. The encoder selected generates 360 pulses per revolution so every mechanical degree is represented by a distinct 9-bit word, thus a 9-bit modulo-360 counter is implemented using three 4029 counter chips. When

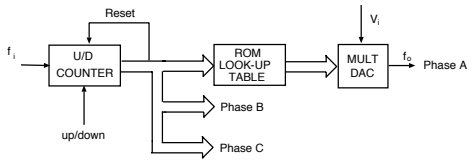

Fig. 2. *The look-up table three-phase sinewave generator*

the rotor motion corresponds to the UP direction, the counter resets to zero every time the maximum (terminal) count of 360 is reached. When counting in the DOWN direction the reset loads a value of 360 on the counter. The digital output from the ROM is passed through a digital-to-analog converter (DAC) so as to obtain an analog sine wave. The amplitude of the output sine wave is controlled by multiplying the DAC output by the voltage v_i, which is obtained from the motor control circuit. Phases B and C have identical ROMs and DACs but their look-up table values are mutually phase-shifted by 120 electrical degrees.

The direction of rotation is determined using a D-flip-flop that compares the phases of pulses coming out of the two channels A and B of the incremental encoder. If channel A is ahead of channel B, for example, the output Q of the flip-flop goes high thereby setting the counter to the UP count mode. Furthermore, under these conditions, the digital number 000000000 is impressed on the jammed input of the counter cascade. Thus when the reset signal C arrives from the encoder and enables the counter presets, zero is jammed through the counters. On the other hand, when the rotor is turning in the opposite direction, the channel B signal is ahead of channel A, and the counters are switched into DOWN mode. Simultaneously, the digital number 101101000 is impressed on the jammed input of the counters, and when the enable reset signal arrives, the number 360 is loaded into the counter.

The digital output from the ROM is passed through a digital-to-analog converter (DAC) so as to obtain an analog sine wave. The amplitude of the output sine wave is controlled by multiplying the DAC output by the voltage v_s which is obtained from the motor control circuit. Phases B and C have identical ROMs and DACs but their look-up table values are mutually phase shifted by 120 electrical dgrees.

V. Hysteresis Current Control

The reference sinewaves that are digitally-generated as described above, are compared with the actual motor currents within a small hysteresis band. The inverter output current is made to follow the reference sine wave within this hysteresis band. Thus the reference current i_{ref} is compared to the actual phase current i_{ph} and if the difference between the two exceeds a certain value δ, corresponding to the hysteresis band, the voltage on the phase is toggled the other way. Table 1 thus gives the switching pattern. The hysteresis comparator is built around a 311comparator chip. The inputs of the comparator are connected one to the output of the reference generator and the other to that of the motor current sensor. The motor stator current sensor itself is implemented using a LOHET

chip which outputs a bipolar signal proportional to the stator current amplitude. This signal is filtered and amplified before it is passed to one of the inputs of the hysteresis comparator.

VI. Modeling the Inverter

In order to simulate the switching logic of the inverter, some assumptions are made. First, the transistors are treated as ideal switches. Next, a dead time of about 20 μs deliberately introduced in the switching-on of each transistor to avoid shoot-through, is neglected here. Thus according to these assumptions, the voltage imposed on the load terminals is either + VDC/2 or DVDC/2 taking the centre of the inverter output as the reference. The inverter's load (i.e. the motor) is assumed to be connected in star.

VII. Motor Model

The simulation is based on the d-q model of the synchronous permanent magnet motor in the rotor reference frame. A simplified model is obtained by neglecting saturation effects together with eddy currents and hysteresis losses. The electromagnetic torque developed by the surface magnet PMSM used for this work has been shown to depend only on the quadrature-axis current. Hence the optimum mode of operation, in terms of torque per stator current, is when the stator current vector is controlled such that it always lies along the q-axis. [2] Under this condition, the direct-axis current component vanishes and the torque becomes directly proportional to the amplitude of the stator current. The dynamics of the motor are then described by the second-order differential equation

$$J\frac{d^2\theta_m}{dt^2} + K_D\frac{d\theta_m}{dt} + T_L = K_T\hat{I}_s \tag{1}$$

where $\hat{I}_s$ is the magnitude of the stator current space vector.

VIII. Power Stage

The power stage is implemented in the standard three-phase bridge arrangement using bipolar transistors, the base drives of which are each isolated and fed from separate independent power supplies. In addition each base drive circuit is isolated from its switching circuit using an optical isolator. To ensure protection from shoot-through, a dead-time of about 25 μs is imposed on the switching signals applied to the base circuits. Overload protection and surge suppression are provided with the help of simple capacitor-type snubber circuits. Furthermore, each transistor is furnished with a freewheeling diode to ensure the safe conduction of the load current during the freewheeling period.

The power stage uses the conventional 6-transistor three-phase bridge configuration. For the purpose of choosing the transistor rating, the inverter is treated as a combination of 6 DC choppers, with each transistor having to be capable of handling the whole of the supply voltage, together with the peak current circulating in one phase of the machine. This means that for transistor voltage and current ratings of V_T and I_T, respectively, the power available to the machine is of the order of about $0.7 - 0.75V_TI_T$ assuming unity-power-factor operation. Obviously if the harmonic contents of the output are lowered, the available power will fall, and for a near-sinusoidal output waveform the value drops down to about $0.6V_TI_T$ for *unity pf* operation.

Thus the DC link voltage is related to the fundamental line-to-neutral voltage, v_{L-N}, by the equation

$$v_{L-N} = M\frac{V_{DC}}{2} \tag{2}$$

where V_{DC} is the DClink voltage and M is the modulation index, which normally lies between zero and unity, except in the case of overmodulation when M can attain values upto 1.18 [6].

The order of the predominant harmonics in a sinusoidally modulated voltage wave is determined by the carrier ratio p, which is not constant in the case of a hysteresis controller based PWM. Thus at high speeds PWM is lost and the inverter changes to a six step operating mode. For a modulation index of unity, the fundamental line-to-neutral voltage becomes $\frac{V_{DC}}{2}$ for a wye-connected load, giving a fundamental rms line voltage of about $0.61V_{DC}$ for the sinusoidal PWM which is less than the corresponding value for the six-step operation.

A. Choice Of Power Semiconductors

The choice of semiconductor switching devices depends not only on the electrical and thermal ratings, but also on the switching frequency, firing-control strategy and other considerations. Figure3 shows the switching capacity and frequency of several types of power semiconductor devices. [5]. Bipolar transistors have found wide applications in the region below 700V, due to their low on-state resistance and relatively short switching times. When speed is the deciding factor, MOSFETS are the favourites. MOSFETS have the added advantage of being high input-impedance devices requiring simple triggering circuits. GTOs are suitable for use in high-voltage high-current applications, but require complex gate-trigger circuits and special protective snubbers. The static induction transistor, SIT, is a relative new comer and it combines high speed and temperature tolerance with very low trigger-current demand, which guarantee its increased application in the future [5].

Considering the low-voltage low-speed nature of the intended application of the inverter, bipolar transistors were chosen for this design. The transistor size and rating were chosen with due consideration to the inductive nature of the load, since the stored energy due to leakage inductances, can produce excessive transient voltages that might exceed the normal values. Specifically two limitations of the bipolar transistor's power handling capability had to be taken into consideration. One is the problem of secondary-breakdown which could occur in either the forward- or reverse-biased conditions. For inductive loads, as is the case here, secondary breakdown would tend to occur in the reverse-biased condition. In order to avoid this, the transistor must be operated within a manufacturer-designated safe operating area, SOA.

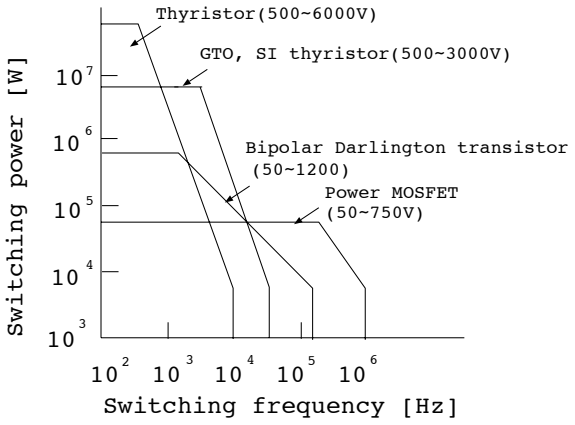

Fig. 3. *Switching capacity of some power devices*

The stored energy level that the transistor can handle normally, specified as $\varepsilon_{s/b}$, is inversely proportional to its switching frequency. Thus for high-frequency application, transistors with low $\varepsilon_{s/b}$ have to be used. This would inevitably mean that snubbers have to be used to absorb the reactive energy and reduce $\frac{dv}{dt}$ accross the device. The other limitation of the transistor's power rating is the junction temperature rise, which has to be curtailed by proper thermal design and heat sinking.

The average output current of the inverter is computed as

$$I_{av} = \frac{I_{rms}}{1.11} \tag{3}$$

The static power loss in a complete half bridge is given by

$$\Delta P_s = I_{av}(((Vce_{sat} - Vd)/2)\cos\phi + (Vce_{sat} + Vd)/2) \tag{4}$$

where Vd is the volt drop accross the freewheeling diode, and Vce_{sat} is the transistor collector-emitter voltage. The choice of free-wheeling diodes is based on the maximum load current and the inverter output voltage. Thus the diodes must be capable of handling the same current as that of the load, and of withstanding a reverse voltage equal to the maximum output voltage.

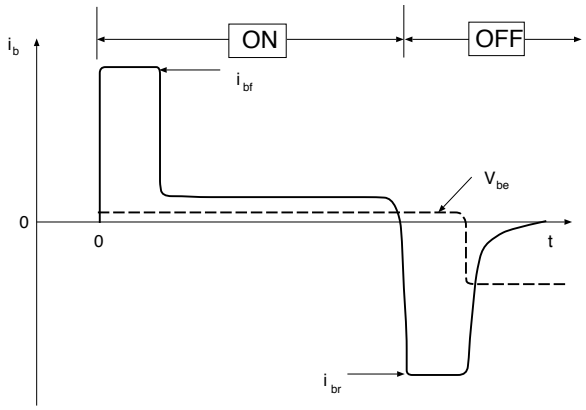

Fig. 4. Ideal bipolar switching transistor base current waveform

IX. Base Circuit Design

The base drive design and performance specification depend very much on the electrical characteristics of the power transistor. Ideally the base current for a switching transistor should have the waveform shown in **figure 4**. Generally a bipolar transistor base drive circuit should possess the following features ;

1) High current pulse at turn-on,
2) Controllable base-current source in the on-state,
3) Anti-saturation circuit,
4) Reverse base current for turn-off,
5) Low base-to-emitter impedance,
6) Base-to-emitter reverse-voltage bias during the off-period.

Often the base drive circuit requires its own electrically-isolated supplies so that, when the emitter is not at ground level, the control signal can be transmitted from the ground-level logic via either a pulse transformer or an opto-isolator. To obtain negative off-bias and reverse base current for faster turn-off, a negative-rail power supply is usually needed. Power dissipation in the base drive can be considerably reduced by using a transistor totem-pole arrangement with antiparallel-connected base-emitter junctions to prevent simultaneous conduction.

The emitter-to-base breakdown voltage rating V_{ebo} specifies the maximum negative rail voltage level. A level of 6-8 V is usually enough, and for supply rail simplicity a ± 6 V supply rail can be chosen. Figure 5 shows the circuit used to drive the base of each of the 6 npn power transistors.

An anti-saturation diode D_{as} which clamps the power transistor collector voltage was used. The collector voltage is given by

$$V_{ce} = V_{beT1} + V_{beTp} - \nu_{Das} \tag{5}$$

The minimum gain β at maximum collector current, I_m, is inturn given by the collector voltage. The diode D_{as} should be a fast-recovery type with a reverse voltage rating in excess of the maximum off-state collector voltage. Its current rating is specified by the maximum collector current I_m, and the respective gains of the transistors Tp and $T1$ that is β and β_1 respectively. Thus the current rating of the anti-saturation diode is given by

$$I_{Das} = \frac{I_m}{\beta\beta_1} \tag{6}$$

The current I_{Das} is the maximum current that bypasses the base input under low collector current conditions. The pnp translation transistor T_t is clamped to reduce saturation delay. Resistor R_4 is needed to limit the base current of T_t. If the base circuit is open collector TTL driven, the current through the resistor R_4 is given by

$$I_{OL} = (V^+ - V_{beTt} - \nu - Db - V_{OL})/R_4 \tag{7}$$

Since $I_{OL} = 40mA$, when $V_{OL} = 0.5V$, for open collector 74 series TTL, the resistor R_4 can be specified. Resistor R_3 helps to speed up the turn-off of transistor T_t, and it is made

as large as possible to ensure that minimal base current is diverted from T_t.

The totem-pole transistors T1 and T2 were chosen to have the following features

1) High gains,
2) Fast-switching capability,
3) Collector current ratings in excess of I_m/β,
4) Collector voltage ratings in excess of $V^+ + \mid V^- \mid$.

Resistor R_{on} determines the main power transistor base current, and its value is given by

$$R_{on} = \frac{(V^+ - V_{ceT1} - V_{beTp})}{I_m/\beta} \tag{8}$$

Its power rating is given by

$$P_{Ron} = \sigma(V^+ - V_{ceT1} - V_{beTp})I_m/\beta \tag{9}$$

where σ is the maximum on-state duty cycle. Capacitor C_{on} provides a short current boost at turn-on and hence speeds up the turn-on process and reduces turn-on losses.

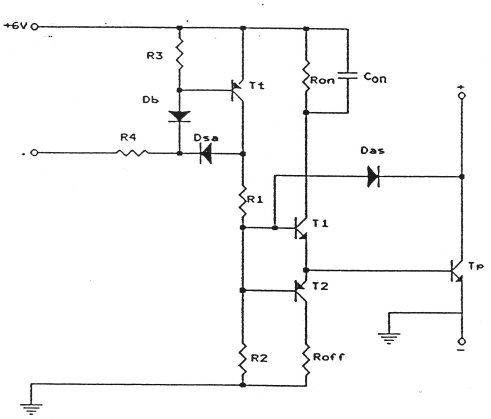

Fig. 5. *Base Drive Circuit*

The resistors R1 and R2 help to bias the bases of the totem pole transistors. The potential at the common base, for an on-condition is given by

$$V_x = V_{beT1} + V_{beTp} \tag{10}$$

The value of resistor R1 can be deduced from the above as

$$R1 = (V^+ - V_x)/I_{R1} \tag{11}$$

where I_{R1} is the current through R1 at the on-state, given by

$$I_{R1} = \frac{I_m}{\beta\beta_1} + \frac{V_x + \mid V^- \mid}{R2} \tag{12}$$

Resistor R2 must be chosen such that it allows a reverse base current that is of the same magnitude as the maximum forward current for fast turn-off. This means that R2 is given approximately by

$$R2 = \frac{\mid V^- \mid - V_{beT2}}{I_c/\beta\beta_2} \tag{13}$$

A small inductance L of the order of microhenrys is placed in the turn-off circuit so as to limit di/dt of reverse base current. Any oscillation of the inductor current is damped by the resistance R_{off}.

X. Base Drive Power Supplies

The isolation of each individual base drive required the implementation of six identical switching mode power supplies. A 555-based square wave generator fed from the common DC supply and operating at 20 KHz is used to control the base of the auxillary transistor inverter. The inverter's output is connected to the isolating transformer T1 which was implemented on a 100W "Ferroxcube" kit which is suitable for high-frequency low-core-loss application. The secondary winding of the transformer is connected to a rectifier bridge. The rectified output of the bridge is filtered and then supplied to the base circuit of a power transistor.

XI. Motor current sensing

A stator-current sensor was implemented using a LOHET chip. The chip outputs a bipolar signal that is proportional to the stator-current amplitude which is filtered and amplified before it is passed to one of the inputs of the hysteresis comparator. The other input of the comparator is connected to the output of the reference generator described above.

XII. Hysteresis Comparator

The hysteresis comparator was built around a 311 comparator chip, as shown in Fig. 6. The hysteresis band is established using the potentiometer VR1. The inputs of the comparator are connected to the outputs of the reference generator and motor-current sensor. Each comparator output is coupled to a transistor firing-circuit via an optical isolator.

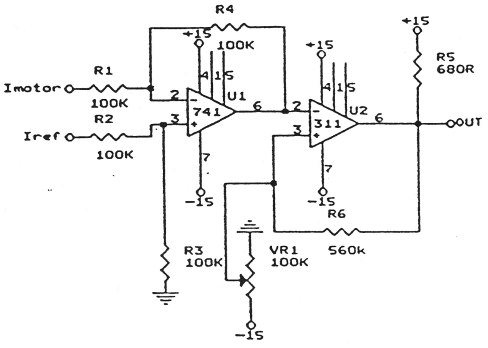

Fig. 6. *Hysteresis Comparator*

XIII. Amplitude and Frequency Calibration

A manually-adjustable reference generator was implemented, and used to calibrate the output amplitude and frequency for given input voltages. The main component of the manually-controlled reference generator is a voltage-to-frequency converter. Pulses from this were passed to a bank

of counters the output of which was then used to address the look-up table ROMs. Thus the frequency is varied by manually changing the input voltage of the voltage-to-frequency converter. The amplitude was varied by changing the reference voltage of the DACs that convert the ROM output values to analog voltage. Results of the calibration were as follows:

Input Voltage [V]	Output Amplitude [V]
0.0	0.0
0.5	0.9
1.0	3.0
1.5	4.1
2.0	5.9
2.5	7.0
3.0	9.0

TABLE II
Reference generator volt/amplitude response

Input Voltage [V]	Output Frequency [Hz]
2	6.2
4	12.5
6	18.6
8	25.1
10	31

TABLE III
Reference generator volt/frequency response

XIV. Conclusion

A brief description of a low-power sinusoidal PWM inverter suitable for variable speed permanent magnet synchronous motor drives has been given. The generation of variable frequency variable amplitude sine wave reference signal using a digital technique based on look-up tables in ROM has been implemented. ACSL simulation has been carried out to study the hysteresis current control of the inverter-motor combination. Results of this simulation have justified the model developed for the system. The inverter was built and used to drive the prototype PMSM in the constant volt/hertz mode for a frequency range from 0 to about 33Hz. Hysteresis current saturation was noticed at frequencies above 20Hz which correspond to motor speeds of more than 400 rpm. There was also a noticeable degree of transistor failure when this speed limit was exceeded. It must be pointed out however, that the inverter's performance when connected to a static (non inductive) load, for various load levels and a full frequency range from 0 to 33Hz was smooth.

References

[1] ALHASSAN, M.H.: 'Permanent Magnet Synchronous Motors in Position Control Systems,' *D. Phil Thesis, University of Sussex, Brighton, 1993*.
[2] https://easyelectriclife.groupe.renault.com/en/outlook/technology/understanding-the-power-output-of-an-electric-motor
[3] BOSE, B.K.: 'A High-Performance Inverter-Fed Drive System of an Interior Permanent Magnet Synchronous Machine,' *IEEE Trans. on Industry Applications, 1988*, **24**, (6), pp. 987-997
[4] CORNELL, E.P.: 'Permanent Magnet AC Motors,' *Conf. Proc. Drives/Motors/Controls, 1983*, pp.102-107
[5] DOTE, Y. and KINOSHITA, S. (-editors): 'Brushless servomotors: fundamentals and applications,' *Clarendon P. Oxford 1990*. 507-515
[6] MURPHY, J.M.D. and TURNBULL, F.G.: 'Power Electronic Control of AC Motors,' *Pegamon, Oxford, 1986*.