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Figure 5 depicts the schematic of a 16x16 block made up of 8x8 blocks. The Urdhva vertical [6] and cross product terms are represented as partial products. The final result is then found using an or and half adder assembly. This multiplier has a power dissipation of 0.18 mW and a propagation latency of 1.71 nsec. This circuit has 618 transistors. a diagram for a 16x16 block made up of 8x8 blocks The Urdhva vertical [6] and cross product terms are represented as partial products. The final result is then found using an or and half adder assembly. This multiplier has a power dissipation of 0.18 mW and a propagation latency of 1.71 nsec. This circuit has 618 transistors.

4. CONCLUSION

Tanner Tool v14.1 is used to simulate the suggested Vedic multiplier (described in section 3). Table 1 compares the proposed multiplier to the Booth radix-4 multiplier and the multiplier in [3]. (2). As seen in the table, this multiplier will aid in the development of faster CPUs in the future. Figure 1 shows a schematic from S Edit (8).

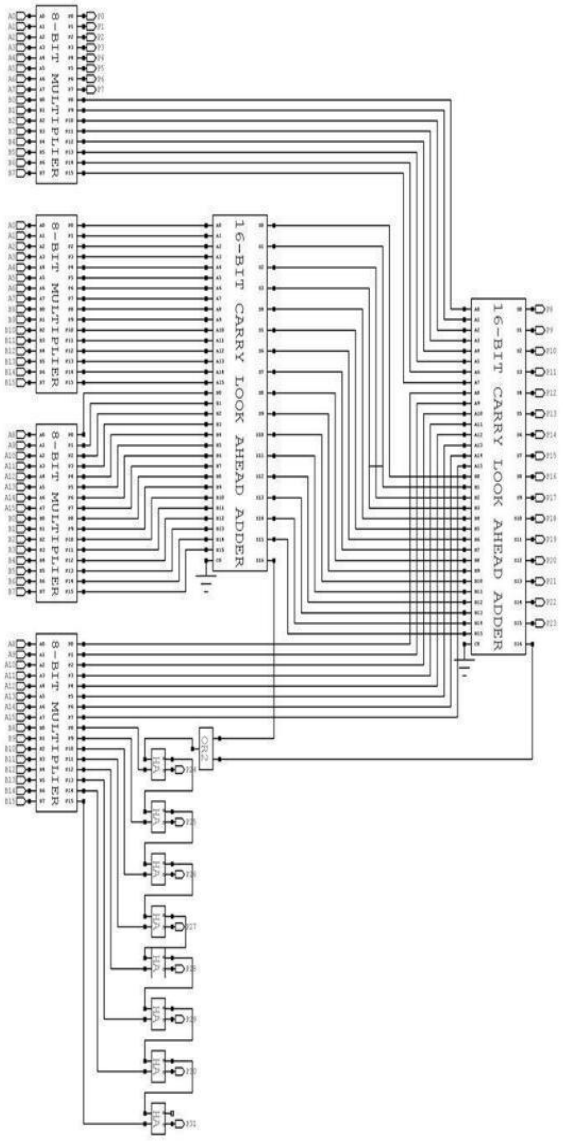

Figure (8): Schematic diagram of 16 bit Multiplier using Urdhva Tiryakbhyam Sutra

Table (2): Table of design comparison of Multipliers

S.No.	Parameters of Comparison	Paper [3] design	Booth algorithm	Proposed design
1	Delay (n sec)	37.668	46.740	27.14865
2	Power Dissipation (m Watts)	29.34	151.34	0.1692638
3	No. of Transistors used	4299	7296	14382

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