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High Speed Low Power 16 bit Multiplier based on Vedic Maths

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ABSTRACT
High-speed parallel multipliers are required in RISCs, DSPs, and graphics accelerators.. Standard ways for creating binary multipliers that are suited for VLSI implementation include array multipliers, Booth multipliers, and Wallace Tree multipliers. The Urdhva Tiryakbhyam (Vertically and Crosswise) Sutra of Vedic Mathematics is used to create a basic digital multiplier (henceforth referred to as Vedic Multiplier in short VM). A new low-power, high-speed multiplier of two binary values (16 bits each) has been devised. On 16nm CMOS technology, an algorithm is presented and implemented. The planned 16x16-bit multiplier consumes 0.17 mW of electricity. The suggested design has a propagation latency of 27.15ns. These findings outperform the Vedic and Booth Multiplier literature in terms of power dissipation and latency.

Keywords
Vedic Multiplier, Urdhva Tiryakbhyam, CMOS Technology, Power Dissipation, Propagation Delay.

1. INTRODUCTION
Between 1911 and 1918, Sri Bharati Krisna Tirthaji (1884-1960) from the Atharva Vedas rediscovered the ancient system of Vedic Mathematics from the Indian Sanskrit books known as the Vedas. According to his study, all of the mathematics is built on sixteen Sutras, or word formulas [1]. These formulas represent how the mind operates in its natural state and may guide the learner to the most suitable solution approach. The Vedic approach may frequently solve tough issues or large quantities of money promptly under the Vedic system. These distinctive and elegant approaches are merely one aspect of a far more systematic system of mathematics than the present one. Vedic Mathematics demonstrates a cohesive and coherent framework of mathematics, using complimentary, straightforward, and simple approaches. It's a unique method of computation based on basic concepts and rules that may be used to answer any mathematical issue, including arithmetic, algebra, geometry, trigonometry, and calculus.

The Urdhva Tiryakbhyam (Vertically Crosswise) Sutra of Vedic Maths is used to suggest a basic 16 bit digital multiplier in this work. This Sutra multiplies two binary values (16 bits apiece). The potential of this technique is that the circuit's power dissipation is 0.17 mW, and the suggested architecture's propagation latency is 27.15ns. These values are better than Vedic and Booth Multiplier power dissipations and delays reported in the literature. Some of the typical methodologies used in the development of binary multipliers that are suited for VLSI implementation include array multipliers, Booth multipliers, and Wallace Tree multipliers.

The method's introduction will be discussed in part 2, along with a description of the Sutra and multiplication processes. Design a 16x16 bit multiplier using fundamental building elements such as 2x2 bit multiplication, 4x4 bit multiplication, and 8x8 bit multiplication in section 3. The comparison of various multipliers is shown in section 4. We'll wrap things up in section 5.

Table (1): Comparison of Different Conventional Multipliers

Parameter	Array Multiplier	Wallace Tree Multiplier	Booth's Multiplier
Operation Speed	Less	High	Highest
Time Delay	More	Medium	Less
Area	Maximum area because it uses a large number of Adders	Medium area because Wallace Tree used to reduce Operands	Minimum area because no of adder/subtractor is small/
Complexity	Less complex	More complex	Most complex
Power Consumption	Most	More	Less
FPGA implementation	Less efficient	Not efficient	Most efficient

2. Introduction to Proposed Technique
2.1 Design Factors of Multiplication: The main aspects to consider while choosing a design for the demand are latency, throughput, area, and design complexity. The length of time that the device's inputs stay stable until the final result shows on the outputs is known as latency. Throughput is the number of multiplications that can be performed in a given length of time.

2.2 Urdhva Tiryakbhyam Sutra[2]

In Vedic Mathematics, the fundamental Sutras and Urdhva Tiryakbhyam Sutra assist in doing practically all number operations quickly and easily[3]. Urdhva Tiryakbhyam is the Sutra that we use in this endeavor (Multiplication).

2.3 Description of Sutra[2]

This is the generic formula for all multiplication situations [3]. The technique of multiplication used is called Urdhva Tiryakbhyam, which means "vertically and across."
Illustration:

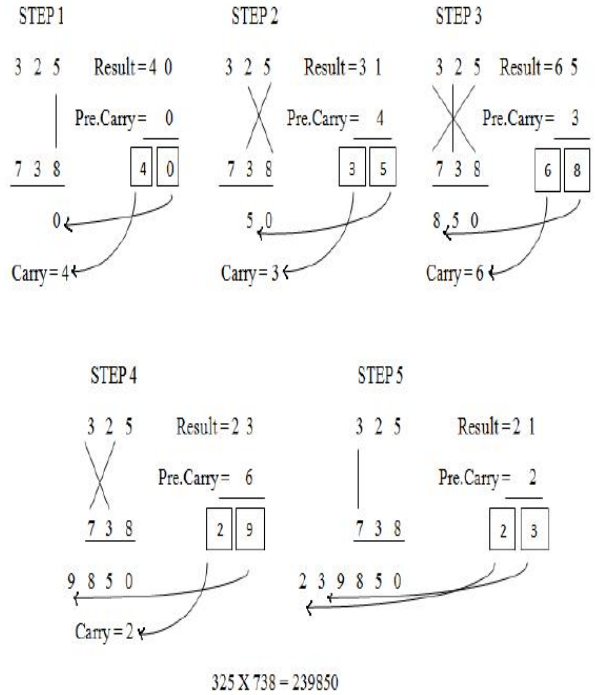

Figure (1): Multiplication of two decimal numbers by Urdhava Tiryakbhyam Sutra [1]

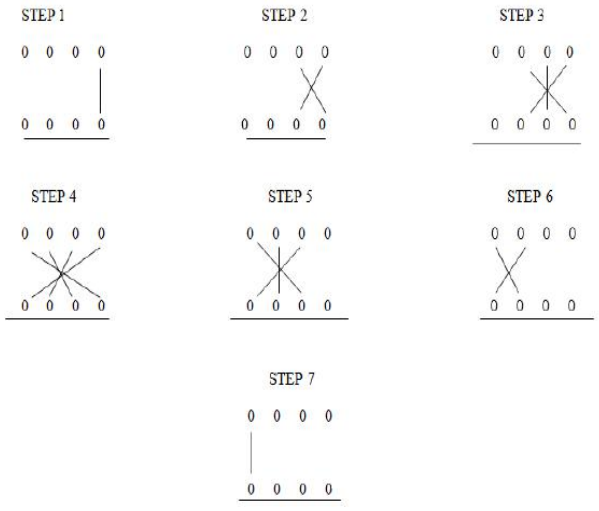

Figure (2): Line diagram for multiplication of two 4 – bit numbers[1].

3. Design Of The 16x16 Multiplier

3.1 The Fundamental Block (2×2 block)

A 22 block is a fundamental block (Basic block) in the design of the proposed Vedic multiplier, as shown in fig 3. This fundamental block's symbol is also shown to be used in a 4 x 4 bit multiplier. In binary multiplication, we know that we basically AND each two bits in a 2-input AND gate[4]. To begin, all vertical bits (LSBs) are ANDed, resulting in the result's LSB. The result is then added using a half adder after we and crosswise bits. The half adder's sum output is the next bit of the result, all the way to the LSB. The carry output is combined with the AND output of the MSBs in a half adder. The result's MSB is the carry of this adder. Figure 4 shows the waveforms of the input and output of a 2-bit multiplier utilizing the Urdhva Tiryakbhyam Sutra [5] of Vedic mathematics. This multiplier has a power dissipation of 23.2 W and a propagation latency of 1.51 nsec. This circuit has 62 transistors.

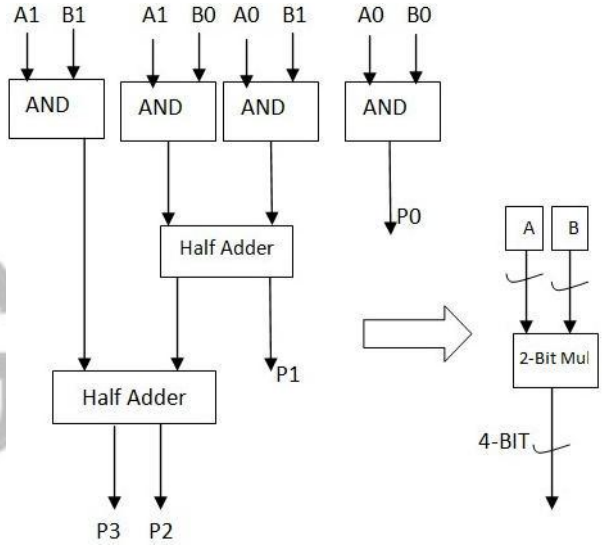

Figure (3): 2-Bit multiplier using Urdhva Tiryakbhyam Sutra & its symbol

Figure (4): Input Output waveforms of 2x2 Bit multiplier

3.2 Design of 4×4 block

The design of 4x4 bricks depicted in fig (5) is a basic, optimized arrangement of 22 blocks. The 2 bits of each 4 bit input will be grouped as the initial stage in the creation of the 44 block. Vertical and crosswise product words will be formed from these pair terms. Each input bit-pair is processed by a separate 22 Vedic block. The Urdhva vertical and cross product terms are represented by the partial products. The final result is then found using an or and half adder assembly. This multiplier has a power dissipation of 0.18 mW and a propagation latency of 1.71 nsec. This circuit has 618 transistors.

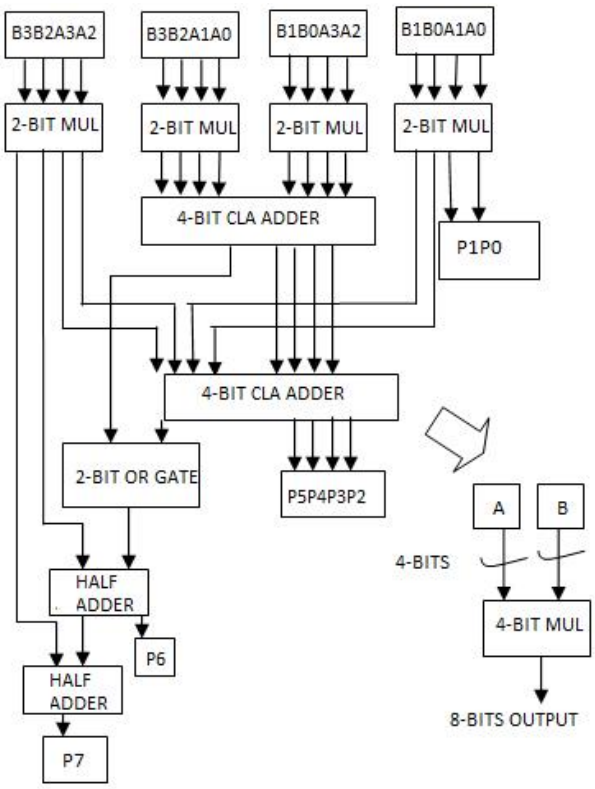

Figure (5): 4-Bit multiplier using Urdhva Tiryakbhyam Sutra & its symbol

3.3 Design of 8×8 block

The design of the 8x8 block is an improved version of the 4x4 block seen in figure 3. The 4 bit (nibble) of each 8 bit input will be grouped as the initial stage in the creation of the 8x8 block. Vertical and crosswise product phrases will be formed by these quadruple words. To make eight partial product rows, each input bit-quadruple is multiplied with a different 4x4 Vedic multiplier. To create final product bits, these partial product rows are ideally added in an 8-bit carry look ahead adder. Figure (6) depicts the schematic for an 8x8 block made up of 4x4 blocks. The Urdhva vertical and cross product terms are represented by the partial products. The final result is then found using an or and half adder assembly. This multiplier has a power dissipation of 0.035mW and a propagation latency of 1.72 nsec. This circuit uses 3222 transistors.

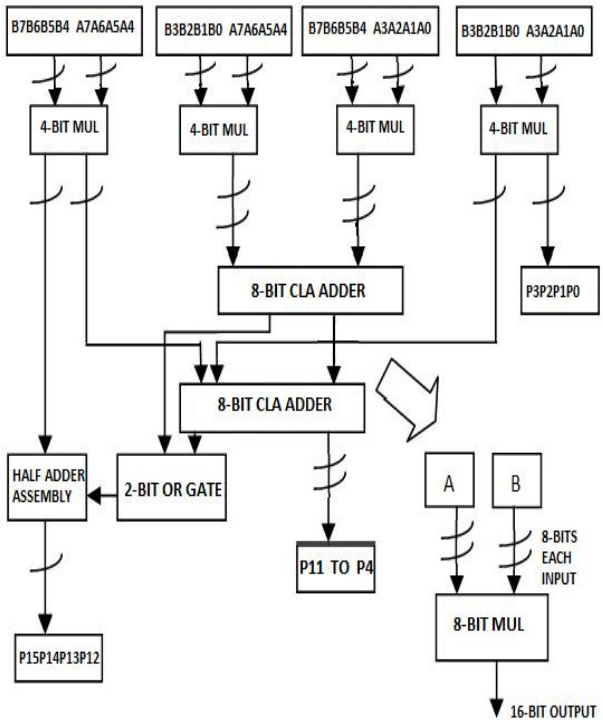

Figure (6): 8-Bit multiplier using Urdhva Tiryakbhyam Sutra & its symbol

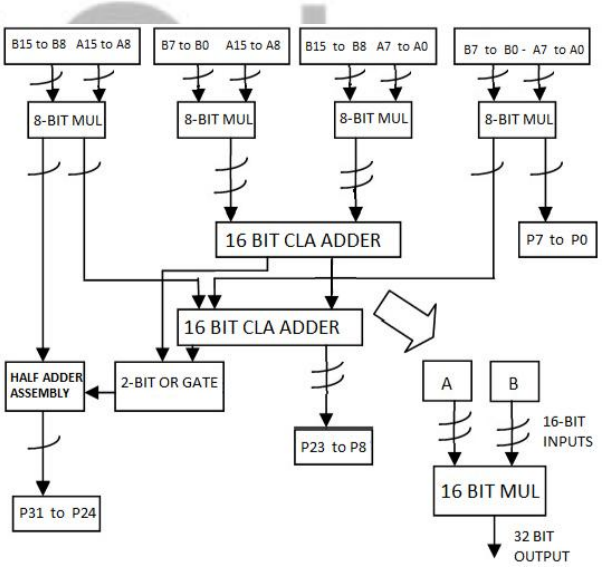

Figure (7): 16-Bit multiplier using Urdhva Tiryakbhyam Sutra & its symbol

3.4 Design of a 16×16 Multiplier

The architecture of the 16x16 block is based on an optimum arrangement of 8x8 blocks as seen in figure (7). The 8 bit (byte) of each 16 bit input will be grouped as the initial stage in the creation of the 16x16 block. Vertical and crosswise product terms will be formed from these lower and higher bytes pairs of two inputs. To make sixteen partial product rows, each input byte is multiplied by an 8x8 Vedic multiplier. To create final product bits, these partial product rows are ideally added in a 16-bit carry look ahead adder.

Figure 5 depicts the schematic of a 16x16 block made up of 8x8 blocks. The Urdhva vertical [6] and cross product terms are represented as partial products. The final result is then found using an or and half adder assembly. This multiplier has a power dissipation of 0.18 mW and a propagation latency of 1.71 nsec. This circuit has 618 transistors. a diagram for a 16x16 block made up of 8x8 blocks The Urdhva vertical [6] and cross product terms are represented as partial products. The final result is then found using an or and half adder assembly. This multiplier has a power dissipation of 0.18 mW and a propagation latency of 1.71 nsec. This circuit has 618 transistors.

4. CONCLUSION

Tanner Tool v14.1 is used to simulate the suggested Vedic multiplier (described in section 3). Table 1 compares the proposed multiplier to the Booth radix-4 multiplier and the multiplier in [3]. (2). As seen in the table, this multiplier will aid in the development of faster CPUs in the future. Figure 1 shows a schematic from S Edit (8).

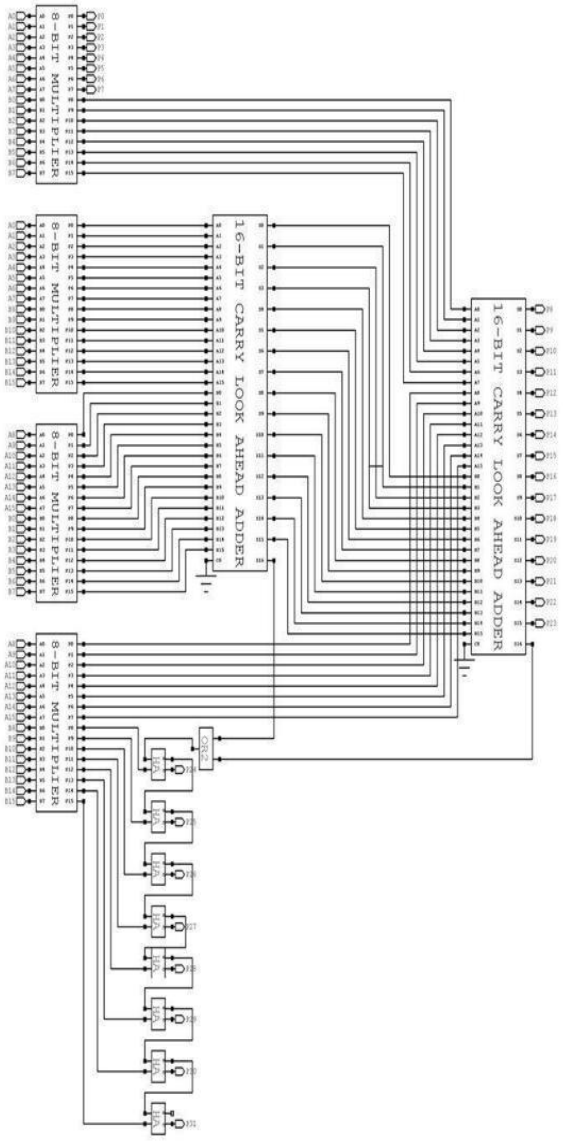

Figure (8): Schematic diagram of 16 bit Multiplier using Urdhva Tiryakbhyam Sutra

Table (2): Table of design comparison of Multipliers

S.No.	Parameters of Comparison	Paper [3] design	Booth algorithm	Proposed design
1	Delay (n sec)	37.668	46.740	27.14865
2	Power Dissipation (m Watts)	29.34	151.34	0.1692638
3	No. of Transistors used	4299	7296	14382

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