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Methodologies for Low Power Physical Design of a RISC Processor

Abhijeet P Shahapurkar
Student
Department of ECE
B. M. S. College Of Engineering
Bengaluru, India
abhijeetp.lvs19@bmsce.ac.in

Dr. Vasundhara Patel K S
Professor
Department of ECE
B. M. S. College Of Engineering
Bengaluru, India
vasu.ece@bmsce.ac.in

***Abstract*— In VLSI circuits, power dissipation is a critical design parameter as it plays a vital role in the performance estimation of the battery operated devices. The decrease in chip size and increase in chip density and complexity increase the difficulty in designing higher performance low power consuming system on a chip. It is very important to have better design approach and power optimization methods with constraint on timing closure and physical verification. The IC's designed today are complex and hence require a good Physical Design optimization and strategies. The primary objective of this project is to obtain a layout that is power efficient and meets timing and DRC requirements. Various power optimization methods are used in Synthesis and Physical Design. Since performance and power consumption are inversely proportional, experiments are conducted to obtain an optimum value which satisfies both these requirements. Each stage on netlist synthesis and layout generation is analyzed in order to find their impact on power and performance. Physical Design is carried out on the 28nm technology node. All the analysis has been done on a functional block which contains both macros and standard cells. The prime objective concentrates on designing an efficient low power functional block in SOC and to conduct a detailed analysis on Power, Performance, Congestion and DRC to check whether the design meets the tape-in quality.**

Keywords— Application Specific Integrated Circuit (ASIC), Design Rule Check (DRC), Clock Tree Synthesis(CTS), Integrated Clock Gating (ICG), Metal Oxide Semiconductor Field Effect Transistor (MOSFET).

I. INTRODUCTION

Power optimization is a very important and challenging step in the application-specific integrated circuit (ASIC) flow and it is a critical success factor of a chip. Especially for RISC processor architecture which includes many numbers of blocks, power optimization is required and should be achieved by managing time. The combination of low-power components in conjunction with low-power design techniques is now more valuable than ever before. As the components become battery-powered, smaller and require more functionality, requirements for lower power consumption continue to increase significantly. In the early days, the major concerns for the VLSI designers were performance, area and cost. Power was considered as the minor concern. In recent day's power has become the major concern due to the successful and efficient development in the field of computer devices and a wireless communication system that requires complex operation with higher calculation speed along with low power consumption. The semiconductor industry has now entered into nanometres technology by reducing the size of transistors which allows us to group more number of transistors in the same die area. It would in-turn reflect in the overall power consumption, number of devices per unit area and ultimately the cost. This reduction in channel length allows manufacturers to include more transistors in essentially the same area. As a result of this, designers can add more features to the design improving the IC performance apart from the improved speed offered by reduction in technology node. Statistically, from each generation to next, performance will increase from approximately 10 to 20 percent [1]. But the scaling in the technology node will be accompanied by a large number of problems in the process of manufacturing which will in turn affect designing. The improvements can be done in power consumption, area utilization and timing depending on the constraints. Timing adjustments and power consumption can be carried out in synthesis as well as place and route stage. IC's designed in the today's world are more complex and hence require a good optimization and strategies in Synthesis and Physical Design. The methods for reducing the power consumption vary application to application. For battery-powered appliances such as laptops, mobile phones, the main objective is to keep lifetime of the battery reasonable and lower packing cost as the battery technology is not improving as fast as the semiconductor technology. In sub-micron technologies, dynamic and leakage power consumption is an important design parameter as it consumes a large portion of total power consumption. Increasing the battery life of portable devices, reducing leakage power and dynamic power appears as the main goal of the VLSI circuit design. Researchers are more focused on developing low-energy components and low-energy design techniques. In low-tech components of less than 0.1 micrometer, leakage power consumption has united the switching function as a major entity in total power consumption [1]. Many low power design methods have been developed to overcome power dissipation, such as multiple voltage thresholds (multi-Vt) to decrease leakage current, clock gating for reducing dynamic power, are well-established and supported by most of the existing tools.

According to a study, 60% of customers' highlighted problem is associated with the power consumption in modern Integrated Circuits [5]. The RISC processor is an exceptional example of a stated problem. The aim of this project is to investigate potential ways to reduce the power of the processor using a variety of low power consumption methods. Power consumption of a metal oxide semiconductor IC is composed of two components dynamic power and static power.

Dynamic power is divided into 2 components i.e., short circuit power and switching power. Short circuit power is consumed when both the nmos and pmos transistors are

turned on simultaneously, and switching power is consumed during charging and discharging of parasitic capacitances. The second component is the static power consumption is caused due to leakage in the standby mode.

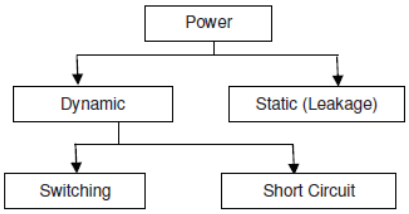

Fig. 1. Power Consumption

$$P_{total} = P_{switching} + P_{short\ circuit} + P_{leakage} \quad (1)$$

II. Physical Design Flow

A. Physical Design Overview

Physical design is conversion of RTL netlist to GDS-II form. In physical design flow, the components like as macros, cells, gates, transistors are represented with geometric representations with fixed shapes and size per fabrication layer.

Physical design flow precisely affects performance, reliability, area, power.

- Performance: A long route between two blocks generates longer delay.
- Reliability: Circuit with more number of vias reduces its reliability.
- Area: Not placing the modules connected near to each other makes them slower as well larger.
- Power: Transistors having small gate lengths have high switching speeds but results in higher leakage current.

B. Stages of Physical Design

Because of its high intricacy, physical design is divided into several stages

- Partitioning: It is breaking complex circuit into small circuits or small modules such that it can be effectively designed and studied separately.
- Floorplanning: This decides shapes and positioning of small circuits and modules, location of input and output ports is also analysed.
- Placement: This decides the locations of all the standard cells and other cells under each block.
- Clock tree synthesis: It is the process of connecting clock signal to all clock pin of the sequential circuits to meet prescribed skew and delay requirements.
- Routing: It is the process that allocates routing resources to the connections.
- Timing-Closure/Signoff: It is the process of optimizing the circuit performance using specialized placement or routing techniques.

III. Power Optimization Methodology and Implementation Details

In VLSI design flow, power optimization is mainly performed at many phases of design flow, i.e., System level (power on/off), Architecture level (Pipelining, Redundancy, data encoding), Circuit level (Logic styles, transistor sizing, Voltage scaling, Voltage islands, Variable V_{DD}, Multiple threshold voltages, Power gating) and Technology level (Threshold reduction, multi threshold voltage). In this paper, power is optimized at circuit level and technology level [2] [3].

TABLE I. Clock Low power techniques used and its tradeoff with Timing/Area and Impact on Design and Implementation

Low Power Technique used	Power Reduction	Timing / Area Penalty	Impact on	
			Implementation	Design
Clock Gating	Medium	Low	Low	Low
Multi Vt	Low	None	None	None
Multi Voltage	High	Low	Medium	High

A. ICG (Integrated Clock Gating) Cells

Clock gating can significantly reduce dynamic power consumption. Dynamic power dissipation is

$$P_{dyn} = C_L\ Vdd^2\ f\ \alpha \quad (2)$$

Where C_L is the Load Capacitance, which is a function of wire length, fan-out and transistor size; V_{dd} is the supply voltage; α is Activity Factor which means how often, on average, the wires switch; f is the clock frequency;

This will reduce unnecessary switching of the cells, as all the part of the chip are not functionally on at all time. Using enable signal we can control the clock propagation in the circuit.

B. Multiple Voltage Supply

As dynamic power is directly proportional to the square of the power supply, reducing the power significantly improves the power performance of the device. But this will impact on timing as gate delay increases due to the reduced threshold voltage. To overcome this problem, high voltage supply can be directly applied only to the timing critical path whereas rest of the chip is supplied with lower voltage. This will ensure that the overall system performance is not affected. Blocks which are having different voltage supplies can be integrated in the chip using level shifters to interface between the different blocks.

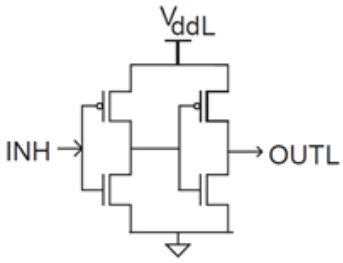

Fig. 2. High to low level shifter

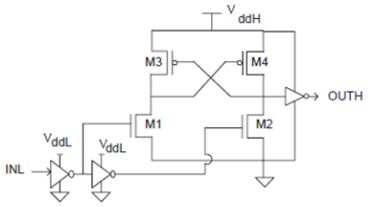

Fig. 3. Low to high level shifter

C. *Voltage Island*

In this technique multiple voltage islands (domains) are used, which allows particular blocks to use less supply voltages than the others and some blocks can be completely turned off only during certain modes of operation. Fig 4 shows and example of Voltage Island in SoC.

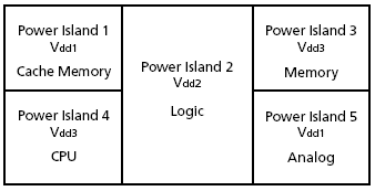

Fig. 4. Voltage Island

D. *Minimize the use of low Vt cells*

The switching speed of the MOSFET depends on its threshold voltage Vt and the device delay reflects as a cell delay. The Low Vt cells are fast in switching and the High Vt cells are slow in switching. The basic step to fix the setup violation is identifying the cell which introduces more delay in the critical path which is of High Vt kind of cell [5]. So, it can be swapped with the same logic cell of Low Vt. By which the path delay is reduced. Hvt cells have less leakage current due to high Vt but they have higher delay than low VT, whereas the low Vt cells are devices, which have less delay, but high leakage power.

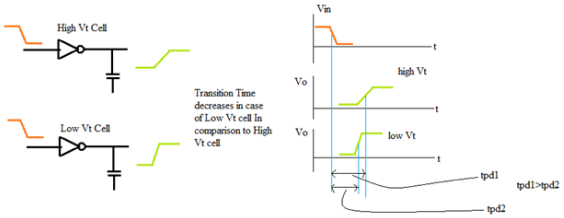

Fig. 5. Timing window for HVT & LVT cells

IV. Result

Optimizing the design with respect to leakage power by macro rearrangement, proper placement of cells and using HVT cells wherever possible in the design meeting timing requirements. Table II shows leakage power optimization in placement stage. Power Reduction is 29.27%.

TABLE II. Leakage Power Optimization in Placement Stage

Leakage Power before Optimization (pW)	Leakage Power after Optimization (pW)
1.64e+10	1.16e+10

Table 3 shows the impact on power after using ICG cells in the design. Total dynamic power is reduced from 2.82e+11 pW to 1.89e+09 pW, hence total power is reduced from 2.93e+11 pW to 7.78e+09 pW.

TABLE III. Clock Gate Impact on power

	Before Inserting Clock Gate	After Inserting Clock Gate
Total Dynamic Power (pW)	2.82e+11	1.89e+09
Total Power (pW)	2.93e+11	7.78e+09

Conclusion

The RTL code for the design is synthesised using Design Compiler Synthesis tool and a technology dependent netlist is generated. With the help of physical aware property, the design is optimised in timing and power by sourcing the floorplan collaterals. The netlist generated at the synthesis output is provided to Physical Design ICC 2 tool, which rigorously optimised the design with the help of different heuristic algorithms. Low power methodologies is implemented in each and every stage from RTL netlist to PnR netlist like clock gating, multi voltage design, multiple voltage islands, and enabling various low power strategies. Both static and dynamic power consumption is reduced used these methods as compared to [5] and [9]. Setup and hold issues are fixed. A best suited method is implemented from all these to get a well optimised low power design. The block is verified through DRC.

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