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Reduced Number of Switches of 31-Level Cascades Multilevel Inverter

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***Abstract*- The output of the sequence associated sub-multilevel-inverter cascaded with the H-bridge inverter so that the resulting output should operate as an inverter in both positive and negative polarities the proposed MLI uses minimum switches. The MLI is being analysed for thirteen level inverter as well as for the thirty-one level inverter. The result of multilevel inverters is compared regarding output voltage current and harmonics. Harmonics to be able determined by using FFT analysis in MATLAB/SIMULINK This research work justifies the performances of cascaded sub multilevel inverter. In the conventional thirteen and thirty-one level cascade sub multilevel inverters, the THD considerably low and induction motor performance**

Keywords—Multilevel inverter, THD, topology, Waveform

I. INTRODUCTION

Industries and utilities have demanded high power alternating current equipment, such as AC drive, STATCOM, UPS & FACTS, and so forth, whose rating reaches to megawatts ranges. In the present scenario, many industrial applications require maximum power; few motor drive and utility grid need intermediate voltage and maximum power level that is in the megawatt The multilevel converter structure is introduced in the year 1975. The label developed the first multilevel inverter in the year 1975 [13] which was a three-level inverter. Subsequently, many MLI structures have proposed, the primary object of the multilevel structure is to get the highest power that is to apply the series association MLI have reduced harmonics and the reduced electromagnetic interference. As we go on enhancing the levels of MLI the output voltage has to add to levels/steps in producing a staircase waveform where we will get a reduced harmonic distortion. However, as we go on rising number of levels of MLI, it rice the amount of power semiconducting devices such as IGBT's, and that is controlled, and hence complexity should also be controlled

II. PROPOSED GENERALISED MULTILEVEL INVERTER

A.MULTILEVEL INVERTER STRUCTURE

In the multi-level topologies, a voltage level of 3 measures the minimum number. Due to the bidirectional switch, the multistage voltage source converter can operate in rectifier mode and inverter mode. That is why we mostly talk about inverters instead of inverters. MLI converter can change its input or output link between various voltage or current levels When the number of levels rises to infinity, THD of the total output move toward zero [29] However, the many of voltage levels is achieved by voltage imbalance issues, voltage blocking supplies, the circuit configuration and circuitry limitations, control complexity, and, of course, energy costs [23], investment and maintenance the more significant number of semiconductor switches in multi-level inverters have a negative impact on reliability and performance. On the other hand, the use of inverters with a small number of semiconductor switches need extensive and expensive L-C filters to limit the insulation loads of motors winding [24], or it can be applied to motors that withstand these limitations. , In industrial applications three large multi-level inverters structures have been used, such as the cascaded H-bridge inverter with take apart direct current sources, the diode-locked inverters and the flying-capacitor inverter.

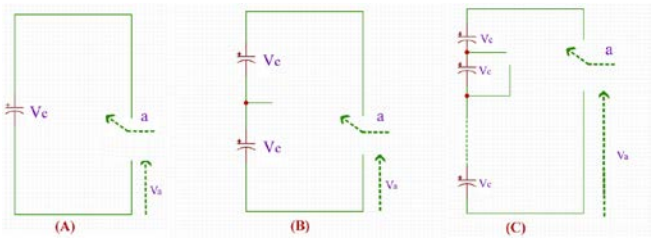

Fig.1. Single phase structure of a multilevel inverter
(a) 2-level (b) 3-level and (c) n-levels

In a multi-stage inverter, the direct current link voltage V_{dc} is gain from each tool that can produce an established direct current source [21]. The series capacitors form an energy

store for the inverter provided that little nodes to which MLI be able to be linked. The capacitors linked in series are mainly more than a few voltage sources with a similar value. Every capacitor voltage V_c is expressed as $V_c = V_{dc} / (m-1)$, where m is the level numbers, and V_{dc} is the maximum continuous voltage.

The figure demonstrates sub- multilevel inverter structure, in this topology, each block is fed with a take apart DC voltage resource. Hence it comprised of n DC voltage sources. DC voltage values for all the blocks are chosen to be same, however different values of DC voltage can also be considered, but for the similar steps of the voltage at the output, same values of DC voltage has been considered and are equal to V_{dc}

It also is noted that in the circuit there are n+ two numbers of switches are connected for sub-multilevel inverter. Unidirectional and bidirectional switches can be used; in this circuit few, unidirectional switches and few bidirectional switches have been used. Line gate bipolar transistors are utilized as unidirectional switches and these IGBT's are connected with an ant parallel diode. In the circuit switches S_1, S_1', S (n+2)/2 and S′(n+2) /2 are used as unidirectional switches and remaining other switches are bidirectional switches [18] . Therefore they will operate in both mode of voltages

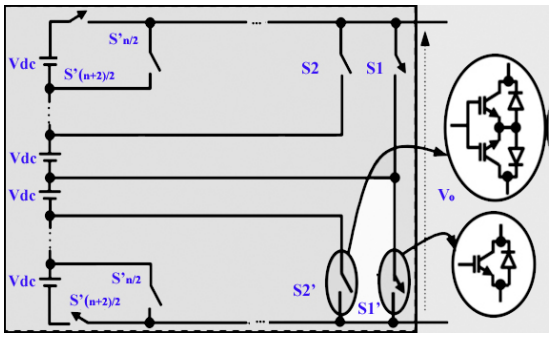

Fig.2 Proposed general sub-multilevel Inverter.

III. Results and Discussion

A. Thirteen Level Inverter

For simulation here, we, have considered a load as R with the worth of 45 Ω. Furthermore, frequency has been 50Hz. These are lots of control technique are available for the multilevel inverter; here we have used the staircase control method. Staircase control method itself indicates that it used because here in this method change of level from one to another occurs once. For the reference voltage, this kind of control method reduces the errors. Shows the multilevel inverter which uses one direct voltage source in all sub-multilevel inverter, n=1 and four series-connected sub-multilevel inverters, m=4. There are four different dc voltage sources 180V, 90V, 45V, 23V have used to get the output voltage of 330V. There is twelve number of IGBT's have been used in this circuit. Here in this topology we have connected four different direct voltage sources, and each of these sources is connected to each sub-multilevel inverters, and this series associated sub-multilevel inverters are connected or cascaded with an H-bridge inverter so that the output should be in both positive and negative polarity.

As shown in the above figure there are twelve switches have been used, some switches are used to generate the positive polarity, and some are used for the negative polarity. Here IGBT's are used as switches.
multicarrier PWM method is used. As shown in the figure, many triangular waves are compared with the reference signal. Multicarrier pulse width modulation method uses one sinusoidal signal as a reference signal and many triangular carrier signals to generate the PWM switching signals. For a 13 level inverter total one less than the number of levels carrier signals are required, hence for a 13 level inverters, 12 carrier signals are required to generate the pulse width modulation switching signals.

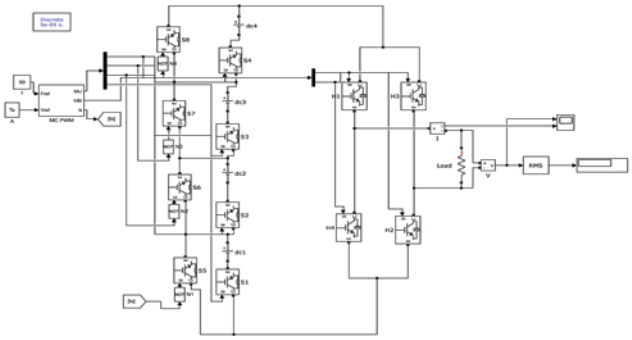

Fig.3.Simulink Model of thirteen level inverter.

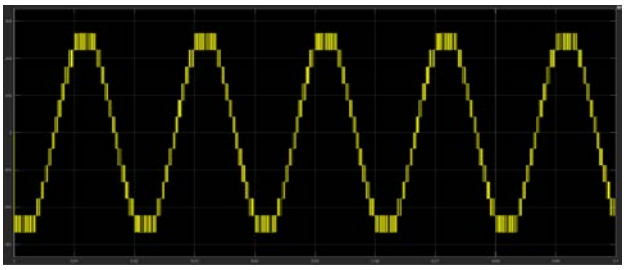

Fig 4 output voltage of thirteen levels cascaded MLI

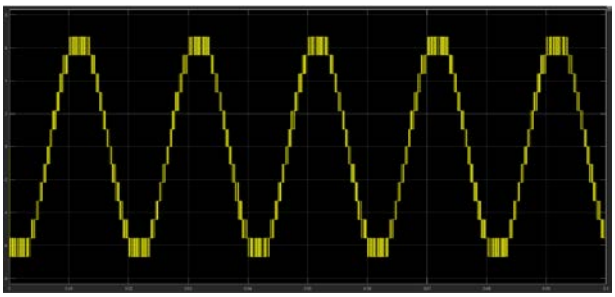

Fig 5 output current of thirteen levels cascaded MLI

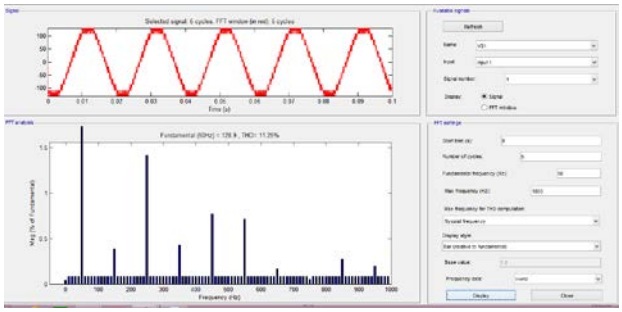

Fig .6 Total Harmonic Distortion of Thirteen level Inverter.

B 31- LEVEL INVERTER

The multilevel inverter which uses one Direct voltage source in every sub-multilevel inverter, n=1 and five series associated sub-multilevel inverter, m=5. There are five different dc voltage sources 180V, 90V, 45V, 23V, 12V have used to get the output voltage of 350V. There is fourteen number of IGBT's have been used in this circuit. Here in this topology we have connected five different direct current voltage sources, and each of these sources is associated to each sub-multilevel inverter, and this series connected sub-multilevel inverters are connected or cascaded with an H-bridge inverter so that the output should be in both positive and negative polarity.

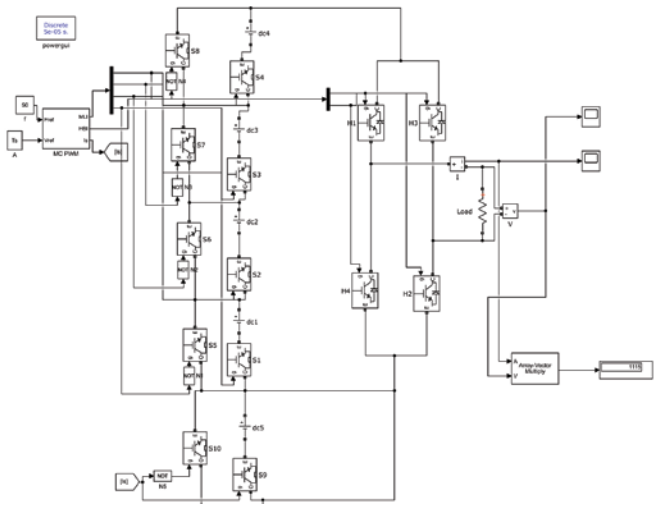

Fig 7 Schematic of 31 level inverter.

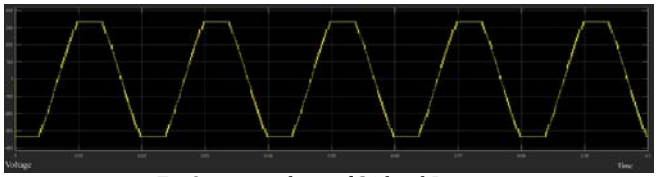

Fig 8 output voltage of 31 level Inverter

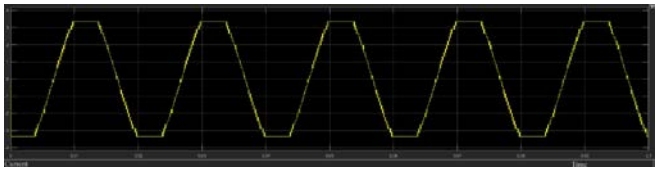

Fig 9 output current of 31 level inverter

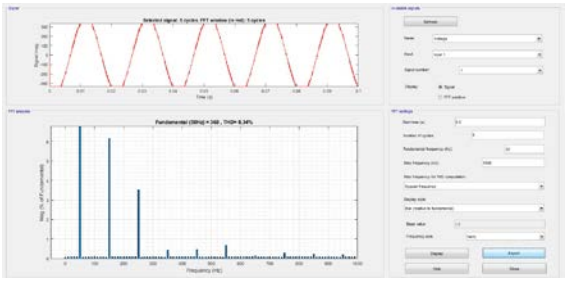

Fig 10 Total harmonic distortion of 31 level inverter

Models have an advantage in reducing the harmonics, which is 8.45% at 368.3V is achieved. The consequences are well within the range of IEEE standards. Moreover, even the proposed model uses a lesser number of switches. Moreover, the power loss of the circuit is less; therefore by just increasing two more switches, we will get the better efficiency and the power factor

IV. CONCLUSION

Table -1 Compression of both MLI

PARAMETERS	13LEVEL INVERTER	31LEVEL INVERTER
No. Of Switches	12	14
Input Voltage	338	350
Output Voltage	128.9	368.3
Output Current	3.3	3.3
Output Power	425.37	1215.39
Harmonics	11.25%	8.45%
Efficiency	38.16	93.48

Comparative study on thirteen level inverters and thirty-one level inverters is made using MATLAB/SIMULINK. Based on the factors of the output voltage, output current, total obtained power and the harmonics, the number of switches used. Proposed models have an advantage in reducing the harmonics, which is 8.45% at 368.3V is achieved. The consequences are well within the range of IEEE standards. Moreover, even model uses a lesser number of switches. Moreover, the power loss of the circuit is less

REFERENCES

[1] J. Hema Latha, Basava Raja Bakara "Modeling and Analysis of 21 Level Cascade Model Multilevel Inverter "*Proceedings of the Second International Conference on Inventive Systems and Control* ISBN:978-1-5386-0807-4; 2018IEEE

[2] MarifDaulaSiddique, Asif Mustafa, AdilSarwar, SaadMekhilef, NoraisyahBinti Mohamed Shah "Single Phase Symmetrical and Asymmetrical Design of Multilevel Inverter Topology with Reduced Number of Switches" *2018 IEEMA Engineer Infinite Conference (eTechNxT)*:978-1-5386-1138-82;2018 IEEE

[3] FatihEroglu, Ali Osman Arslan, Mehmet Kurtoglu, Ahmet Mete Vural. "Generalized adaptive phase-shifted PWM for single-

phase seven-level cascaded H-bridge multilevel inverters",*2018 5th International Conference on Electrical and Electronic Engineering (ICEEE)*, 2018

[4] Torkaman, Ali Mosallanejad. "Minimizing switching losses in cascaded multilevel inverters by proper switching array selection", *2018 9th Annual Power Electronics, Drives Systems and Technologies Conference (PEDSTC)*, 2018.

[5] SubhashreeChoudhury, SamikhyaNayak, Tara Prasanna Dash, PK Rout. "A comparative analysis of five level diode clamped and cascaded H-bridge multilevel inverter for harmonics reduction", *2018 Technologies for Smart-City Energy Security and Power (ICSESP)*, 2018

[6] Junfeng Liu, Jialei Wu, Jun Zeng. "Symmetric/Asymmetric Hybrid Multilevel Inverters Integrating Switched-Capacitor Techniques", *IEEE Journal of Emerging and Selected Topics in Power Electronics*, IEEE 2018.

[7] MasoudBarmala, DaryoushNazarpour, SajjadGolshannavaz, Reza Choupan. "A new structure for multilevel inverters intended to increase the operational reliability", *2018 9th Annual Power Electronics, Drives Systems and Technologies Conference (PEDSTC)*, 2018.

[8] AmirhoseinGohari, EbrahimAfjei, HosseinTorkaman, Ali Mosallanejad. "Minimizing switching losses in cascaded multilevel inverters by proper switching array selection",*9th Annual Power Electronics, Drives Systems and Technologies Conference (PEDSTC)*, 2018

[9] Richard Castillo, Bill Diong, Preston Biggers. "Single-phase hybrid cascaded H-bridge and diode-clamped multilevel inverter with capacitor voltage balancing", *IET Power Electronics,2017*

[10] Himansu N Chaudhari " Comparison of symmetrical and asymmetrical cascaded current source multilevel inverter" *International Journal of Research in Engineering and Technology*, 2013

[11] Sabari Nathan, L., S. Karthik, and S. Ravi Krishna. "The 27-level multilevel inverter for solar PV applications", *IEEE 5th India International Conference on Power Electronics (IICPE)*, 2012.

[12] Elsheikh, Maha G., Mahrous E. Ahmed, EmadAbdelkarem, and Mohamed Orabi. "Single phase five-level inverter with less number of power elements", *2011 IEEE 33rd International Telecommunications Energy Conference (INTELEC)*, 2011

[13] M. Chithra, S.G. BharathiDasan. "Analysis of cascaded H bridge multilevel inverters with photovoltaic arrays", *2011 International Conference on Emerging Trends in Electrical and Computer Technology*, 2011

[14] G. P. Adam, O. Anaya-Lara, G. M. Burt, D. Telford, B. W. Williams, and J. R. McDonald, "Modular multilevel inverter: pulse width modulation and capacitor balancing technique," *IET Power Electron.*, vol. 3, no. 5, pp. 702–715, 2010

[15] M. Manjrekar and T. A. Lipo, "A hybrid multilevel inverter topology for drive application," *in Proc. Appl. Power Electron. Conf.*, 1998, vol. 2, pp. 523–529

[16] FaridKhoucha, MounaSoumiaLagoun, AbdelazizKheloui, and Mohamed El HachemiBenbouzid, "A Comparison of Symmetrical and Asymmetrical Three-Phase H-Bridge Multilevel Inverter for DTC Induction Motor Drives"*IEEE TRANSACTIONS ON ENERGY CONVERSION*, VOL. 26, NO. 1, MARCH 2011

[17] C.kamalakannan, L.pdmasuresh, subhran susekhar dash" power Electronics and renewable systems" *proceedings of ICRERES,2014*

[18] P Mamatha, ChallaVenkatesh," Performance Improved Multilevel Inverter with Selective Harmonic Elimination"*International Conference on Recent Trends in Electrical, Electronics and Computing Technologies*, 978-1-5090-6266-9/17 2017 IEEE

[19] Nupur Mittal, Bindeshwar Singh, S.P Singh, Rahul Dixit, and Dasharath Kumar" Multilevel Inverters: A Literature Survey on Topologies and Control Strategies" *2nd International Conference on Power, Control and Embedded Systems*, 978-1-4673-1049-9/12 2012 IEEE

[20] Jih-Sheng L a, Fang ZhengPeng" MultilevecloNverters- A Newb Reedo F Power Converters"*ConJRec. Ieee*, 0-7803-3008-0195,1995 IEEE

[21] T.Poompava, A.Chitra, C.Srinivas, K.Giridharan"Meticulous Analysis of Induction motor drive fed from a Nine-level Cascade H-Bridge inverter with a level shifted Multicarrier PWM"*2013 International Conference on Smart Structures & Systems (CSS-2013), March 28 - 29,2013, Chennai, India,978-*1-4673-6240-5/02 2013 IE

[22] L.padnasuresh, surbhran susekhar dash, bijayaketan panigrahi "artificial intelligence and evolutionary algorithms in engineering system" *proceeding of ICAEES 2014, volume 1*

[23] Anshuman Shukla, Arindam Ghosh, Avinash Joshi" Flying Capacitor Multilevel Inverter and its Applications in Series Compensation of Transmission Lines" *IEEE Power Engineering Society General Meeting, IEEE 2004*

[24] Bhuvaneswari, Hari Kumar" Flying Capacitor Multilevel Inverter and its Applications in Series Compensation of Transmission Lines" *IEEE Power Engineering Society General Meeting, IEEE 2004,10.1109/ICGCCEE.2014.6922440*

[25] A. Reddiprasanna1, P. Chandrasekhar2, G. Jayakrishna"A Novel Seven Level Multilevel Inverter With Photovoltaic Cell ", *International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering*, Vol. 2, Issue 10, October 2013

[26] Leon M. Tolbert, FangZhengPeng, Thomas G. Habetler"Multilevel Converters for Large Electric Drives "; *Ieee Transactions On Industry Applications, Vol. 35, No. 1, January/February 1999*,0093–9994/99 1999 IEEE

[27] Shweta Gautam, Rajesh Gupta" Generalized Hysteresis Current Controller for Three-level Inverter Topologies *'*, *IEEE International Symposium on Industrial Electronics*, 978-1-4673-0158-9/12/2012 IEEE

[28] Won-Kyo Lee, Soo-Yeon Kim, Jong-Su Yoon, Doo-Hyun Baek"A Comparison of the Carrier-based PWM techniques for Voltage Balance of Flying Capacitor in the Flying Capacitor Multilevel Inverter ", *IEEE Transactions on Industrial Electronics Volume: 65, Issue: 4, April 2018,*

[29] DasareddyMohanreddya and TenapalliGowriManoharb"Harmonics Mitigation and Switching loss reduction using Cascaded Multilevel Based Half Bridge and Full Bridge Inverter System"*International Journal of Current Engineering and Technology ISSN 2277 – 410 6*, Vol.3, No.2 (June 2013)

[30] Himanshu N Chaudhari, Dhaval A Patel, Dhrupa M Patel, Maulik A Chaudhari" Comparison Of Symmetrical And Asymmetrical Cascaded Current Source Multilevel Inverter ", *Ijret: International Journal of Research in Engineering and Technology, Volume:* 02 Issue: 09 Sep-2013

[31] JanardhanKavaliArvind Mittal"Analysis of various control schemes for minimal Total Harmonic Distortion in cascaded H-bridge multilevel inverter"*Journal of Electrical Systems and Information Technology*, Volume 3, Issue 3, December 2016, Pages 428-441

[32] A. Reddiprasann a, P. Chandrasekhar, G. Jayakrishna"A Novel Seven Level Multilevel Inverter With Photovoltaic Cell ", *International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering*, Vol. 2, Issue 10, October 2013

[33] RadhaSree. K, Sivapathi.K, Vardhaman.V, Dr.R.Seyezhai"A Comparative Study of Fixed Frequency and Variable Frequency Phase Shift PWM Technique for Cascaded Multilevel Inverter"*Engineering Research and Applications (IJERA) ISSN: 2248-9622*, Vol. 2, Issue4, July-August 2012, pp.2025-2030

[34] MasoudBarmala, DaryoushNazarpour, SajjadGolshannavaz and Reza Choupan"A New Structure for Multilevel Inverters Intended to Increase the Operation Reliability"*2018 9th Annual Power Electronics, Drives Systems and Technologies Conference*,978-1-5386-4699-1/18/2018 IEEE

[35] Marcelo Pérez, José Rodríguez, Jorge Pontt, Samir Kouro" Power Distribution in Hybrid Multi-cell Converter with Nearest Level Modulation" *IEEE International Symposium on Industrial Electronics,1-4244-0755-9/07/2007 IEEE*