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TIMING OPTIMIZATION TECHNIQUE'S FOR CONTROLLER'S ARCHITECTURE

Abstract: Performance variation has become an increasingly critical design objective as VLSI technology scales into the nanometer domain wherein parametric variations are inevitably significant. The decrease in chip size and increase in chip density and complexity increase the difficulty in designing higher performance low power consuming system on a chip. It is very important to have better design approach and timing optimization methods with constraint physical verification. The IC's designed today are complex and hence require a good Physical Design optimization and strategies. The primary objective of this project is to obtain a layout that is power efficient and meets timing and DRC requirements. Various timing optimization methods are used in Synthesis and Physical Design. Since performance and power consumption are inversely proportional, experiments are conducted to obtain an optimum value which satisfies both these requirements. Each stage on netlist synthesis and layout generation is analysed in order to find their impact on power and performance. Physical Design is carried out on the 28nm technology node. All the analysis has been done on a functional block which contains both macros and standard cells.

Chapter 1: Introduction

Very large scale integration is processes were many transistors are embedded on a single silicon semiconductor chip. The semiconductor industry has now entered into nanometres technology by reducing the size of transistors which allows us to group more number of transistors in the same die area. Following the trends in the semiconductor industry from the beginning, the only requirement for the improvement in performance of an IC has been reduction in the channel length. It would in-turn reflect in the overall power consumption, number of devices per unit area and ultimately the cost. This reduction in channel length allows manufacturers to include more transistors in essentially the same area. As a result of this, designers can add more features to the design improving the IC performance apart from the improved speed offered by reduction in

technology node. Statistically, from each generation to next, performance will increase from approximately 10 to 20 percent. But the scaling in the technology node will be accompanied by a large number of problems in the process of manufacturing which will in turn affect designing. The improvements can be done in power consumption, area utilization and timing depending on the constraints. Timing adjustments and power consumption can be carriedoutinsynthesisaswellasplaceandroutestage.

Timing analysis is organized analysis of a digital circuit to verify timing constraints of by components are met. This means that you are trying to meet all setup time and hold time.

The primary goal of place and route tool is to determine where to place each and every gate. To do this, the tool has to provide with a detailed floorplan with which it can model the design. It included the aspect ratio, utilization, I/O placements etc. In block level design, the interfaces and block shape are decided on a broader level as it depends on the adjacent blocks and the overall SOC structure. While some are partition specific.

A lot of heuristic algorithms are used to decide how to place and where to place such that prior to placement itself it will determine ways to tackle routing congestions and wiring delay and place accordingly. Typical focus will be given to minimize critical path delay. Efforts are taken to resize gates and insert buffers. More often resynthesizing will also be considered. Although meeting timing requirements gets precedence, tool will try to reduce power and area by giving optimum routing option for noncritical paths. Other important aspect of Place and route stage is clock tree synthesis. Clock propagation consumes majority of power in an IC. By properly planning clock tree synthesis we can save overall power in this front.

Chapter 2: Problem Statement

Time is very important parameters for any processor architecture, so time optimization should be done at each and every stage during physical design. In any design we have to look for the timing critical paths because these critical paths are also responsible for increased power in the circuit. Especially for the controller architecture which includes many numbers of blocks, timing optimization is required and should be achieved. The primary objective of the project is to obtain a layout which meets timing and DRC requirements. Techniques for making negative margin paths to positive margin are explained here. Various optimizations methods like cell

swapping, buffer insertion, increase or decrease in driving cell are used in Synthesis and Physical Design.

Chapter 3: Timing Design Flow of Static Analysis

In VLSI timing performed flow. Static each path timing checking design.

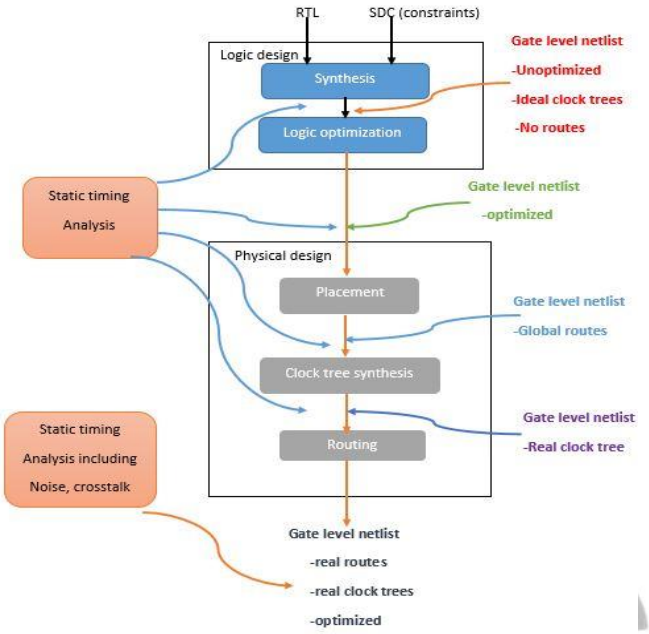

Fig 1: Design Flow

design flow, the static analysis is mainly at many phases of design Timing analysis checks of the design for any violations without the functionality of the

When design is synthesized from Register transfer level to Gate level STA analysis is used to check timing requirements of the design. Static timing analysis carries out logic optimization to recognize the critical timing paths. Repetitive iterations of STA analysis can be

done after logic level optimization to check whether there are any failing paths still remaining which are required to be optimized to check the violating paths in the design.

In the beginning of physical design stage such as floorplan and placement, the clock is considered as clock is reaching to all flipflop at same time. Later in the CTS stage clock tree is constructed and STA analysis is performed to check timing.

In PD flow static timing analysis is performed at each and every phase to recognize the worst delay paths in design. In logic design stage, there is no physical information related to the placement of macros and std cells since the interconnect is ideal. So to get the length of interconnect wire load model is used which gives RC interconnect length based on fanout of cell. In placement stage macros and standard cells are connected by interconnect metal traces. The parasitic of RC components of the metal gives the delay and power dissipation in the design. In global route phase the tool used to calculate routing length is used to calculate the capacitance and resistance which are required to calculate wire delays.Before routing stage coupling effect are not considered to obtain RC values. This is done after detailed routing where actual RC values are obtained from extraction tool and coupling is also analyzed.

Chapter 3: Physical Design Flow

Physical design is conversion of RTL netlist to GDS-II form. In physical design flow, the components like as macros, cells, gates, transistors are represented with geometric representations with fixed shapes and size per fabrication layer

Physical design flow precisely affects performance, reliability, area, power.

- Performance: A long route between two blocks generates longer delay.
- Area: Not placing the modules connected near to each other makes them slower as well larger.
- Reliability: Circuit with more number of vias reduces its reliability.
- Power: Transistors having small gate lengths have high switching speeds but results in higher leakage current.

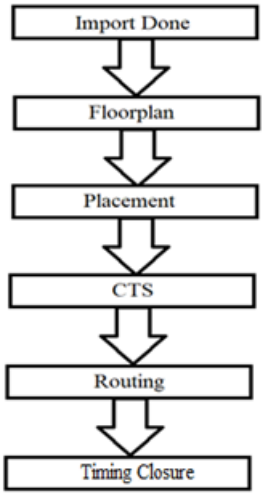

Fig 2: Physical Design Flow

Because of its high intricacy, physical design is divided into several stages

Partitioning: It is breaking complex circuit into small circuits or small modules such that it can be effectively designed and studied separately.

Floorplanning: This decides shapes and positioning of small circuits and modules, location of input and output ports is also analyzed.

Placement: This decides the locations of all the standard cells and other cells under each block.

Clock network synthesis: It is the process of connecting clock signal to all clock pin of the sequential circuits to meet prescribed skew and delay requirements

Routing: It is the process that allocates routing resources to the connections.

Timing-Closure/Signoff: It is theprocess of optimizing the circuit performance using specialized placement or routing techniques.

Chapter 4: Proposed Methodology

4.1 Techniques For Setup Violations

- Reduce the amount of buffering in the path.

Buffers are added in any path to improve the cell delay during the process of synthesis. These buffers in the data path are one of the major reasons to the increase the delay in the violating paths. So these buffers can be reduced in the specific path to fix the setup violation of the path.

➢ Replace buffers with 2 Inverters place farther apart

To reduce the stages interconnect delay a single buffer can be replaced with multiple inverters for various stages. So here every inverter will work as a repeater and improve the signal transition time in every stage as shown in Fig 4. But there should be a tradeoff between the number of inverters and the signal transition time in interconnect.

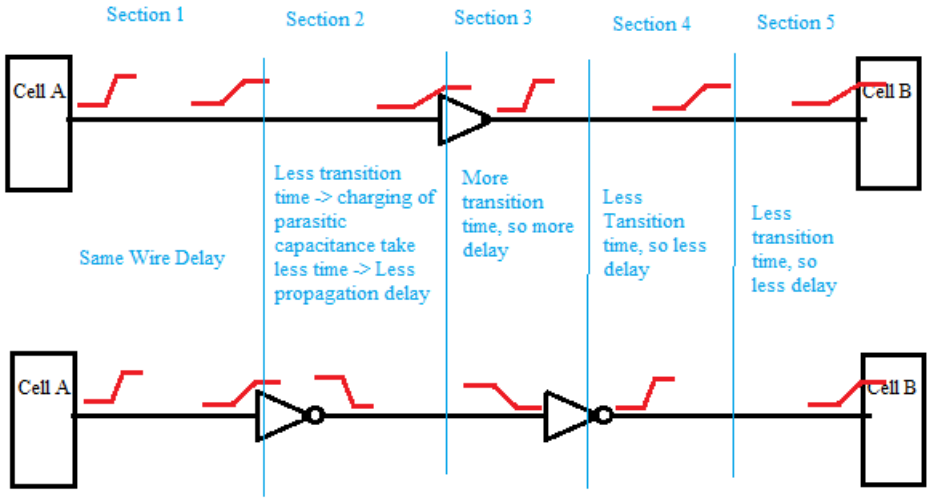

Fig 4: Replace buffer with inverter

➢ Swap cells with lower-Vt.

The switching speed of the MOSFET depends on its threshold voltage Vt and the device delay reflects as a cell delay. The Low Vt cells are fast in switching and the High Vt cells are slow in switching. The basic step to fix the setup violation is identifying the cell which introduces more delay in the critical path which is of High Vt kind of cell. So, it can be swapped with the same logic cell of Low Vt. By which the path delay is reduced.

Negative effect: Leakage current/power also increases.

➢ Upsize the drive strength of data-path logic gates:

The cell having high driving strength of the cell will reduce time to charge the cell to its load capacitance. So, if there setup time violation in any path and there is a specific cell with high delay then these cells can be replaced by the high driving strength of same type logic cell to meet the setup timing. For example assume the 2-input NOR is gate the driver cell with the strength

of 1 X introduces more delay to drive the load then in this case the cell which is the cause for setup violation in the path can be replaced by the cell of strength 2X 2-input NAND gate of same logic from the same technology library.

- Insert Buffers to make interconnect short:

The signal transition for long interconnects will keep on increase as the interconnect length increases. So insert some buffers as a repeater which will improve the signal transition and reduces the interconnect delay.

Negative Effect: Area will increase and increase in the power consumption.

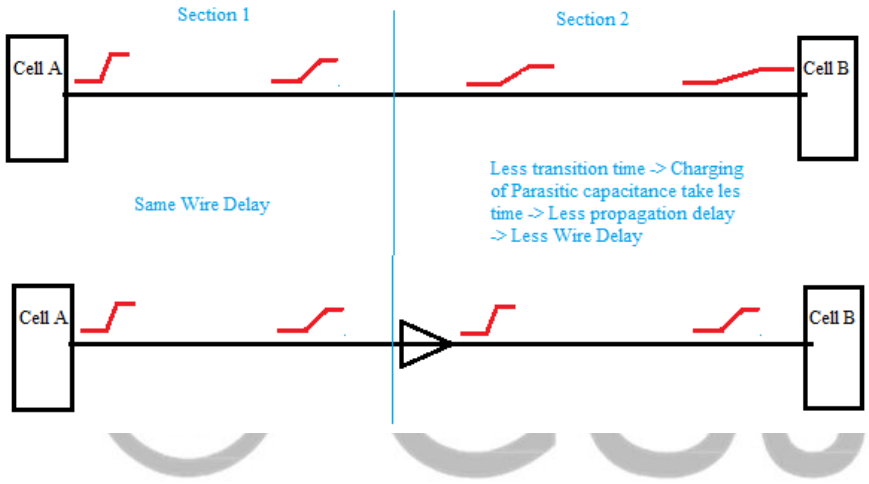

Fig 6: Insert Buffers

- Changing the clock skew:

Positive skew aids to improve the setup slack. So to fix setup time violation another technique is done by considering the clock path is varying the clock skew between launching flip-flop to the capturing flip-flop. This can be achieved either by increasing the capture clock path delay or reducing the launching path delay. But doing this the setup slack and hold slack of other flipflop which are can be changed.

4.2 Techniques For Reducing Hold Violations

- Insert delay elements:

In any path having hold timing violations can be solved by inserting the delay cells in the data path. So, the data path increases and avoids the date to reach in shorter duration.

- Downsizing the driving strength of logic cells in data path:

The hold violation is fixed by increasing the cell delay this is done by reducing the drive strength. For example a 2-input AND gate is a driver cell with the strength of 2X. It can be replaced by the 1X 2-input AND gate from the same technology library to increase the delay. The reason is because of its lower drive strength (1X) compared to 2X cell will increase its delay.

- Swap cell with higher Vt:

Low Vt cells are fast in switching and High Vt cells are slow n switching. So, to fix hold violation swapping the Low Vt cells with High Vt cells of the same kind which introduces the delay in the hold violation path and the slack becomes positive.

- Changing the clock skew:

The positive skew reduces the hold time violations whereas the negative skew improves hold time violations. If the violating path is data path then we can reduce the capturing clock latency or increase latency of launching clock. But this technique should not be used until required as it may affect the timing paths starting or ending at this flipflop.

- Detoured routing:

Detoured routing technique can be adopted instead of inserting the delay elements as it will add load to driving cell since it provides some additional net delay which effectively increases the data-path delay.

Chapter 5: Results

Analyzed the critical timing paths of the design and applied STA to those critical paths ensuring that the design functionality is not changed.

The setup and hold margin is tabulated with respect to reference design.

Timing Path		Previous Design	Current Design
MAX/setup	WNS in ps	-7.24	-1.75

	Number of negative paths	8699	248
MIN/hold	WNS in ps	-2.48	-0.13
	Number of negative paths	3499	159

Chapter 6: Conclusion

In VLSI digital circuits are each version of designs has a particular frequency. Withevery new generation of microprocessor, the operation frequency changes. The RTL codefor the design is synthesized using Design Compiler Synthesis tool and a technology dependent netlist is generated. With the help of physical aware property, the design isoptimized in timing and power by sourcing the floorplan collaterals. The netlist generated atthe synthesis output is provided to Physical Design ICC 2 tool, which rigorously optimized the design with the help of different heuristic algorithms.

Timing optimization methodologies is implemented in every stage from RTL netlist to PnR netlist inthe paths were the setup and hold time is violated. Both setup time and hold time is Metusing these methods. A best suited method is implemented from all these to get a welloptimized design. The block is verified through DRC. Experiments for timing optimizationis performed with efficient gain in setup margin and hold margin.

Chapter 7: Future Work

Each new project will be an improvement over its predecessor. This is achieved by adding newer RTL features and further technology scaling. This requires more efforts in terms of performance optimization and better quality checks.

Use of additional timing optimization techniques can be used in the design to reduce the setup and hold violations.

Other important factors are noise and its effect on the signals. Extensive work can be done in this field to achieve immunity from noise. Moreover, accounting for onchip variation to get best picture of timing and making an OCV aware clock tree could be another research area that could be looked into. Timing of the critical paths, speedpath analysis and debug are other factors that could be a plan of future works.

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